Nokia Customer Care
2118 (RH-77)
Mobile Terminal

Baseband Description and Troubleshooting

Issue 01 04/2005

Contents

Page

Introduction

The baseband module is a CDMA single-band engine based on the DCT4 architecture and consists of three ASICs: Universal Energy Management cost effective (UEMC), Universal Phone Processor (UPP8M4.2), and a 64 megabit FLASH.

The baseband architecture supports a power-saving function called *sleep mode*. Sleep mode shuts off the VCTCXO, which is used as the system clock source for both the RF and the baseband. During sleep mode, the system runs from a 32 kHz crystal and all the RF regulators (VR1A, VR1B, VR2, ... VR7) are off. The sleep time is determined by network parameters. Sleep mode is entered when both the MCU and the DSP are in standby mode and the normal VCTCXO clock is switched off. The mobile terminal is waken up by a timer running from this 32 kHz clock supply. The period of the sleep/wake up cycle (slotted cycle) is 1.28N seconds, where N= 0, 1, 2, depending on the slot cycle index.

2118 supports standard Nokia 2-wire and 3-wire chargers (ACP-x and LCH-x). However, the 3-wire chargers are treated as 2-wire chargers. The PWM control signal for controlling the 3-wire charger is ignored. UEMC ASIC and EM SW control charging.

BL-5C Li-ion battery is used as main power source and has nominal capacity of 850 mAh.

Baseband and RF Architecture

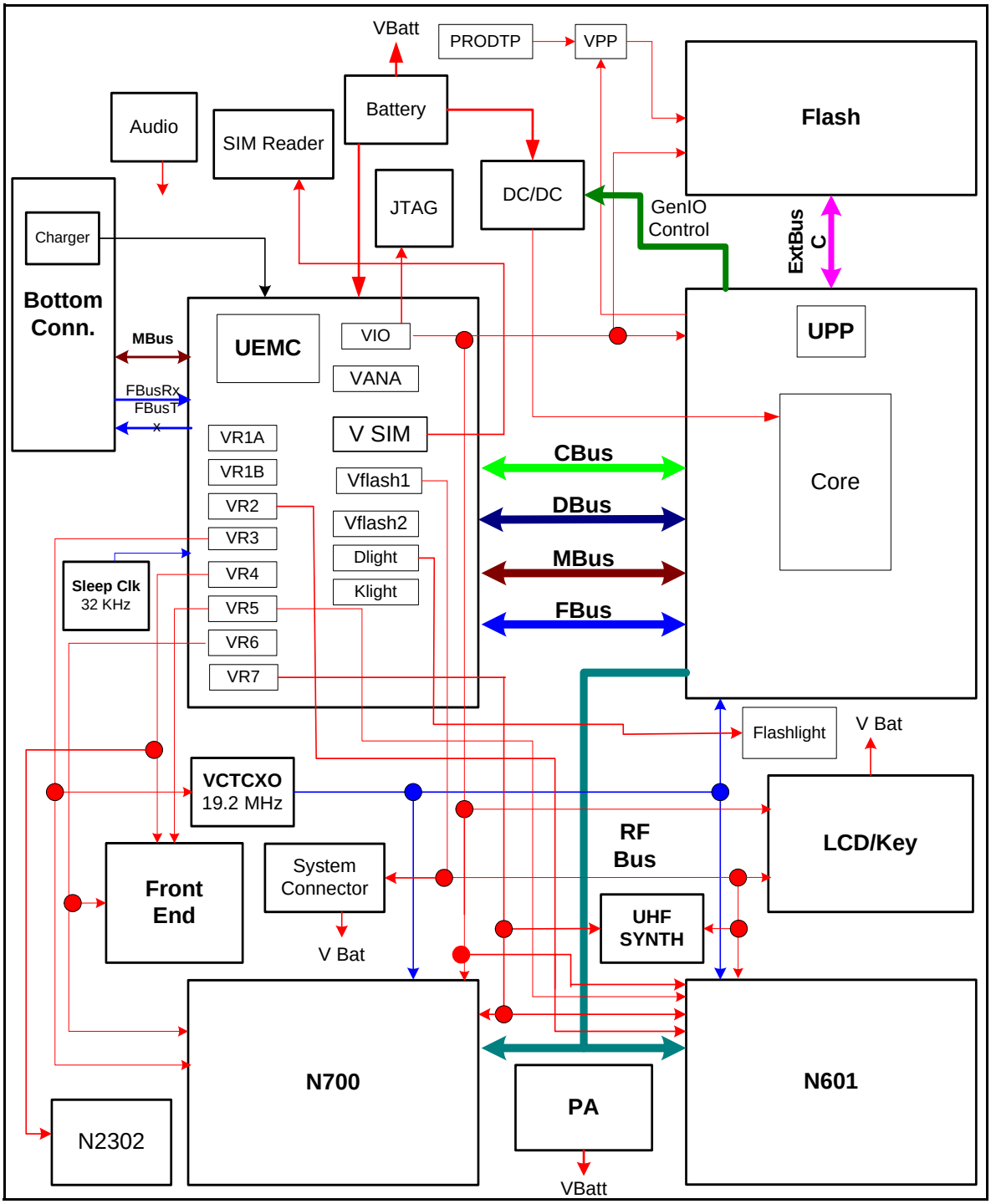


Figure 1: Power distribution

Power Up and Reset

Power up and reset are controlled by the UEMC ASIC. The baseband can be powered up in the following ways:

- Pressing the Power button, which means grounding the PWRONX pin of the UEMC
- Connecting the charger to the charger input
- Initiating the RTC Alarm, when the RTC logic has been programmed to give an alarm

After receiving one of the above signals, the UEMC counts a 20 ms delay and then enters reset mode. The watchdog starts, and if the battery voltage is greater than Vcoff+, a 200 ms delay is started to allow references (etc.) to settle. After this delay elapses, the VFLASH1 regulator is enabled. Then, 500 us later, the VR3, VANA, VIO, and VCORE are enabled. Finally, the Power Up Reset (PURX) line is held low for 20 ms. This reset (PURX) is sent to the UPP. Resets are generated for the MCU and the DSP. During this reset phase, the UEMC forces the VCTCXO regulator on — regardless of the status of the sleep control input signal to the UEMC. The FLSRSTx from the UPP is used to reset the flash during power up and to put the flash in power down during sleep. All baseband regulators are switched on when the UEMC is powered on. The UEMC internal watchdogs are running during the UEMC reset state, with the longest watchdog time selected. If the watchdog expires, the UEMC returns to the power off state. The UEMC watchdogs are internally acknowledged at the rising edge of the PURX signal to always give the same watchdog response time to the MCU.

The following timing diagram represents the UEMC start-up sequence from reset to power-on mode.

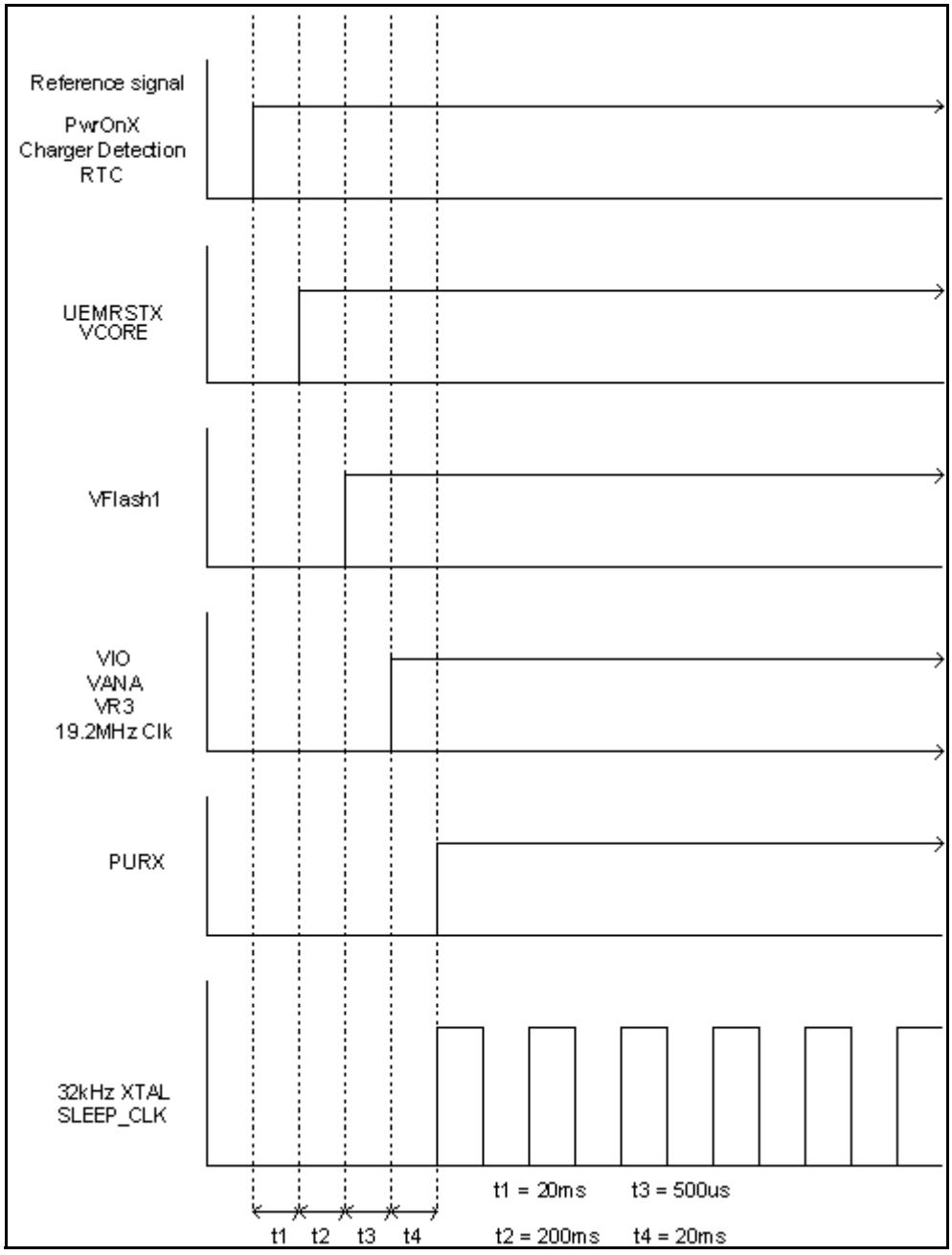


Figure 2: Power-on sequence and timing

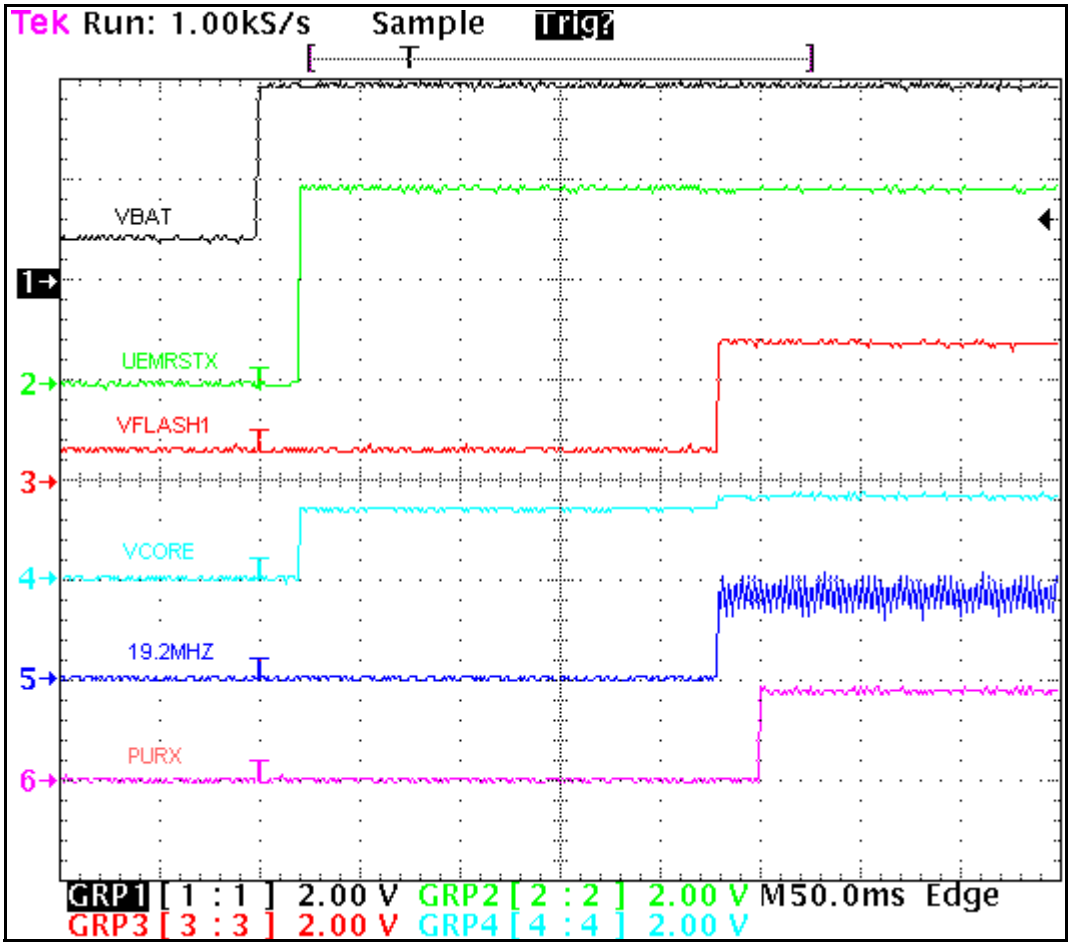


Figure 3: Measured power-on sequence and timing

Power Up – Power Key

When the power key is pressed, the UEMC enters the power-up sequence. Pressing the power key causes the PWRONX pin on the UEMC to be grounded. The UEMC PWRONX signal is not part of the keypad matrix. The power key is only connected to the UEMC. This means that when pressing the power key an interrupt is generated to the UPP that starts the MCU. The MCU then reads the UEMC interrupt register and notices that it is a PWRONX interrupt. The MCU reads the status of the PWRONX signal using the UEMC control bus (CBUS). If the PWRONX signal stays low for a certain time the MCU accepts this as a valid power-on state and continues with the SW initialization of the baseband. If the power key does not indicate a valid power-on situation, the MCU powers off the baseband.

Power Up – Charger

In order to be able to detect and start charging in cases where the main battery is fully discharged (empty) and hence UEMC has no supply (NO_SUPPLY or BACKUP mode of UEMC), charging is controlled by start-up charging circuitry.

Whenever the VBAT level is detected to be below the master reset threshold (V_{MSTR-}), charging is controlled by START_UP charge circuitry. Connecting a charger forces the

VCHAR input to rise above the charger detection threshold (VCH_{DET+}) and by detection, start-up charging is initiated. The UEMC generates 100 mA constant output current from the connected charger's output voltage. The battery's voltage rises at it charges, and when the VBAT voltage level is detected to be higher than master reset threshold limit (V_{MSTR+}), the START_UP charge is terminated.

Monitoring the VBAT voltage level is done by charge control block (CHACON). A MSTRX='1' output reset signal (internal to the UEMC) is given to the UEMC's reset block when the VBAT>V_{MSTR+} and the UEMC enters into the reset sequence.

If the VBAT is detected to fall below V_{MSTR} during start-up charging, charging is cancelled. It will restart if a new rising edge on VCHAR input is detected (VCHAR rising above VCH_{DET+}).

Power Up - RTC Alarm

If the mobile terminal is in power-off mode when the RTC alarm occurs, the wake-up procedure intiates. After the baseband is powered on, an interrupt is given to the MCU. When an RTC alarm occurs during active mode, the interrupt is generated to the MCU.

Power Off

The baseband switches to power-off mode if any of following occurs:

- Power key is pressed
- Battery voltage is too low (VBATT < 3.2 V)
- Watchdog timer register expires

The UEMC controls the power-down procedure.

Power Consumption and Operation Modes

In power-off mode, the power (VBAT) is supplied to the UEMC, vibra, LED, PA, and PA drivers. During this mode, the current consumption is approximately 35 uA.

In the sleep mode, both processors (MCU and DSP) are in stand-by mode. The mobile terminal enters sleep mode only when both processors make this request. When the SLEEPX signal is detected low by the UEMC, the mobile terminal enters sleep mode. The VIO and VFLASH1 regulators are put into low quiescent current mode, VCORE enters LDO mode, and the VANA and VFLASH2 regulators are disabled. All RF regulators are disabled during sleep mode. When the SLEEPX signal is detected high by the UEMC, the mobile terminal enters ACTIVE mode and all functions are activated.

Sleep mode is exited either by the expiration of a sleep clock counter in the UEMC or by some external interrupt (generated by a charger connection, key press, headset connection, etc.).

In sleep mode, the VCTCXO is shut down and the 32 kHz sleep clock oscillator is used as a reference clock for the baseband.

In ACTIVE mode, the mobile terminal is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. There are several sub-states in the active mode depending on the mobile terminal present state of the mobile terminal, such as burst reception, burst transmission, if the DSP is working, etc.

In active mode, SW controls the UEMC RF regulators: VR1A and VR1B can be enabled or disabled. VSIM can be enabled or disabled and its output voltage can be programmed to be 1.8 V or 3.3 V. VR2 and VR4—VR7 can be enabled or disabled or forced into low quiescent current mode. VR3 is always enabled in active mode and disabled during Sleep mode and cannot be control by SW in the same way as the other regulators. VR3 will only turn off if both processors request to be in sleep mode.

CHARGING mode can be performed in parallel with any other operating mode. A BSI resistor inside the battery pack indicates the battery type/size. The resistor value corresponds to a specific battery capacity. This capacity value is related to the battery technology.

The battery voltage, temperature, size, and charging current are measured by the UEMC, and the charging software running in the UPP controls it.

The charging control circuitry (CHACON) inside the UEMC controls the charging current delivered from the charger to the battery and mobile terminal. The battery voltage rise is limited by turning the UEMC switch off when the battery voltage has reached 4.2 V. The charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

Power Distribution

In normal operation, the baseband is powered from the mobile terminal's battery. The battery consists of one Lithium-Ion cell capacity of 850 mAh and some safety and protection circuits to prevent harm to the battery.

The UEMC ASIC controls the power distribution to the whole mobile terminal through the BB and RF regulators excluding the power amplifier (PA), which has a continuous power rail directly from the battery. The battery feeds power directly to the following parts of the system:

- UEMC
- PA
- Vibra
- Display
- Keyboard lights

The heart of the power distribution to the mobile terminal is the power control block inside the UEMC. It includes all the voltage regulators and feeds the power to the whole system. The UEMC handles hardware power-up functions so the regulators are not powered and the power up reset (PURX) is not released if the battery voltage is less than 3 V.

The 2118 baseband is powered from five different UEMC regulators (see Table 1).

Table 1: Baseband Regulators

Regulator	Maximum Current (mA)	Vout (V)	Notes
VCORE	300	1.35/1.05	Power up default 1.35 V and 1.05 V in Sleep Mode.
VIO	150	1.8	Enabled always except during power-off mode
VFLASH1	70	2.78	Enabled always except during power-off mode
VFLASH2	40	2.78	Enabled only when data cable is connected
VANA	80	2.78	Enabled only when the system is awake (Off during sleep and power off-modes)
VSIM	25	3.0	Enabled only when SIM card is used

Table 2 includes the UEMC regulators for the RF.

Table 2: RF Regulators

Regulator	Maximum Current (mA)	Vout (V)	Notes
VR1A	10	4.75	Enabled when cell transmitter is on
VR1B	10	4.75	Enabled when the transmitter is on
VR2	100	2.78	Enabled when the transmitter is on
VR3	20	2.78	Enabled when SleepX is high
VR4	50	2.78	Enabled when the receiver is on
VR5	50	2.78	Enabled when the receiver is on
VR6	50	2.78	Enabled when the transmitter is on
VR7	45	2.78	Enabled when the receiver is on

The charge pump that is used by VR1A is constructed around the UEMC. The charge pump works with the CBUS (1.2 MHz) oscillator and gives a 4.75 V regulated output voltage to the RF.

Clock Distribution

RFClk (19.2 MHz Analog)

The main clock signal for the baseband is generated from the voltage and temperature controlled crystal oscillator VCTCXO (G500). This 19.2 MHz clock signal is generated at the RF and is fed to N700 pin 18 (TCXO_IN). N700 then converts the analog sine waveform to a digital waveform with a swing voltage of 0 tot 1.8 V and sends it to the UPP from pin 16 at N700 (19.2 Out) to the UPP pin M5 (RFCLK).

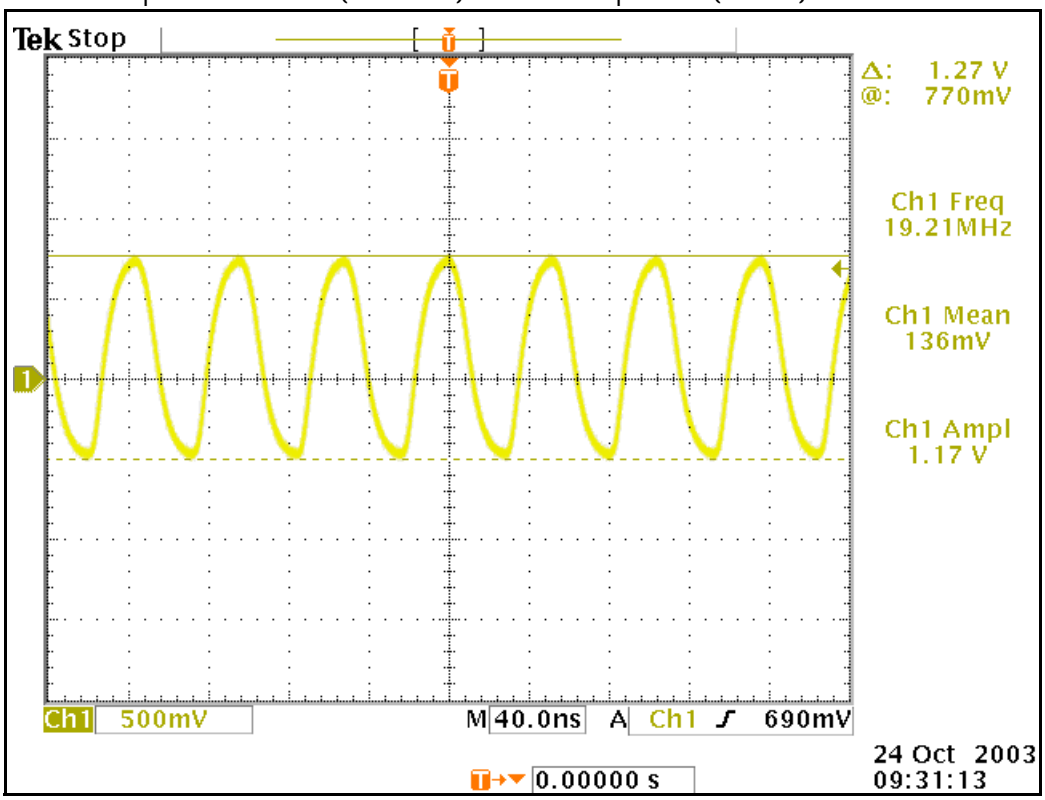


Figure 4: Waveform of the 19.2 MHz clock (VCTCXO) going to the N700 ASIC

Figure 5 shows the RFCLK signal for the UPP.

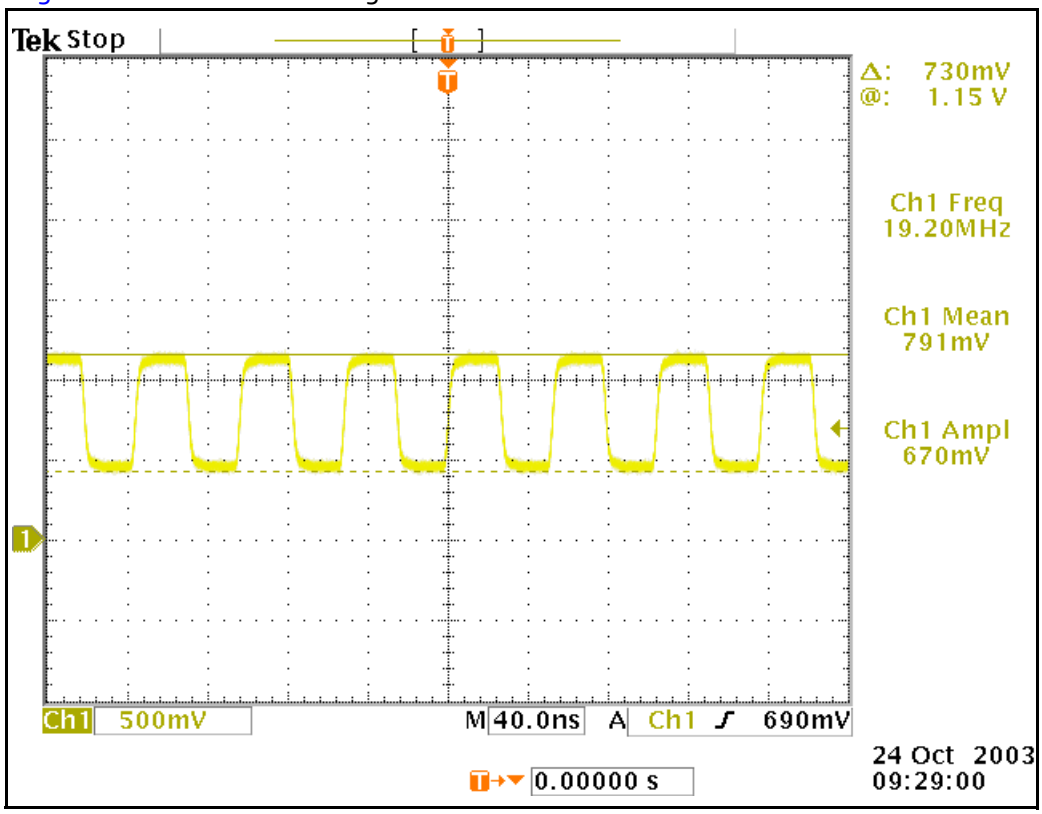


Figure 5: Waveform of the 19.2 MHz Clk going to the UPP for N700 ASIC at C711

RFConvClk (19.2 MHz digital)

The UPP distributes the 19.2 MHz internal clock to the DSP and MCU, where the software multiplies this clock by seven for the DSP and by two for the MCU.

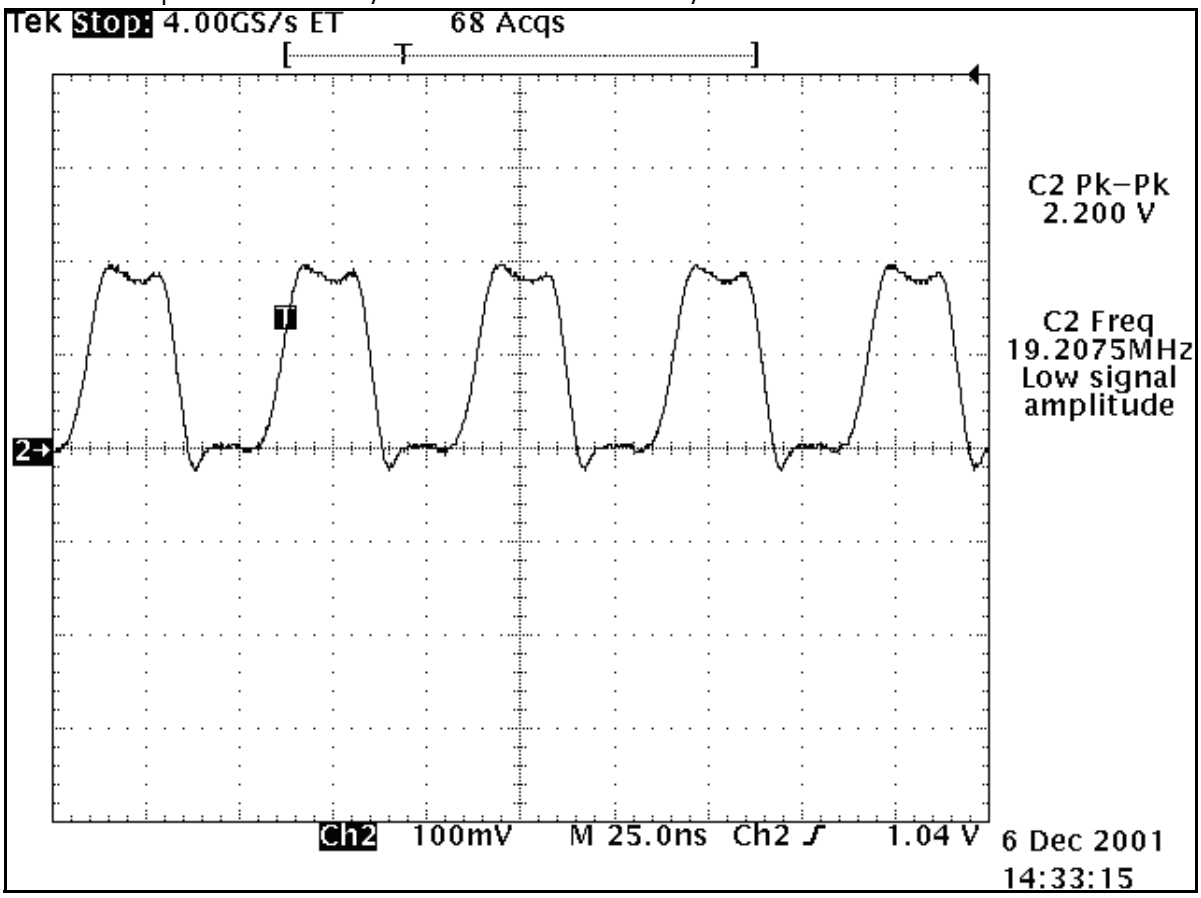


Figure 6: RFCovCLk waveform

CBUS Clk Interface

A 1.2 MHz clock signal is used for CBUS, which is used by the MCU to transfer data between the UEMC and UPP.

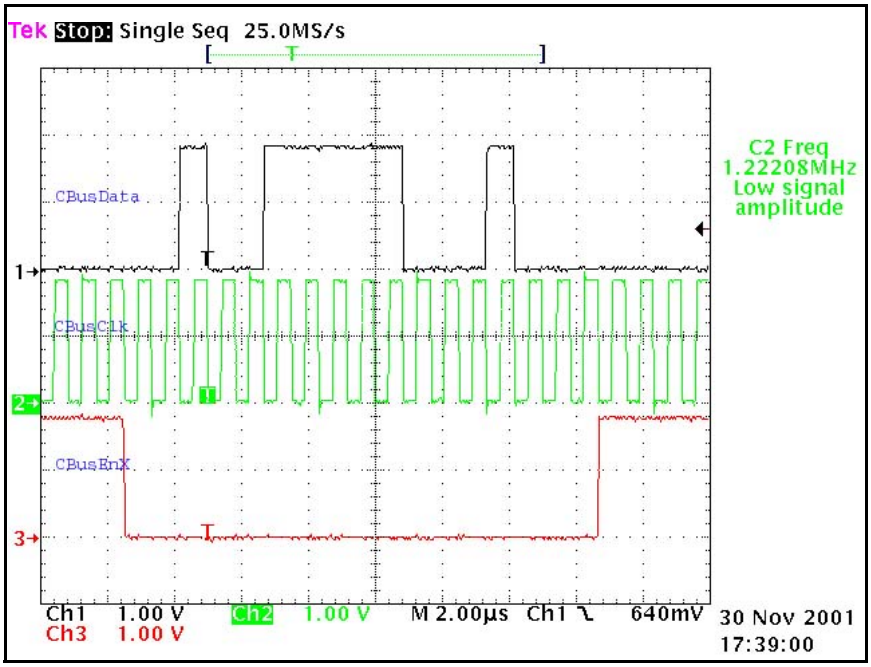


Figure 7: CBUS data transfer

DBUS Clk Interface

A 9.6 MHz clock signal is used for DBUS, which is used by the DSP to transfer data between the UEMC and UPP.

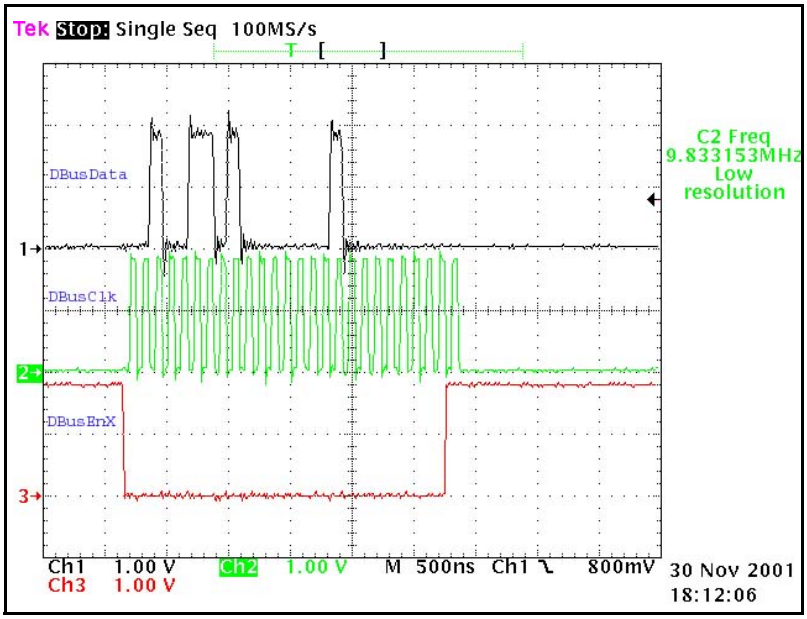


Figure 8: Dbus data transferring

The system clock is stopped during sleep mode by disabling the VCTCXO power supply (VR3) from the UEMC regulator output by turning off the controlled output signal SleepX from the UPP.

SleepCLK (Digital)

The UEMC provides a 32 kHz sleep clock for internal use and to the UPP, where it is used for sleep mode timing.

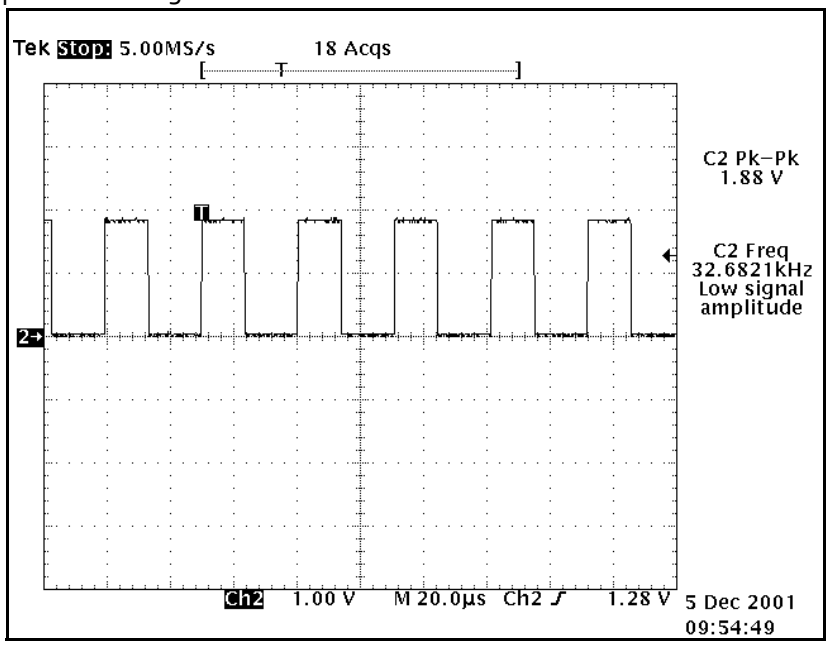


Figure 9: 32 kHz Digital output from UEMC

SleepCLK (Analog)

When the system enters sleep mode or power off mode, the external 32 KHz crystal provides a reference to the UEMC RTC circuit to turn on the mobile terminal during power off or sleep mode.

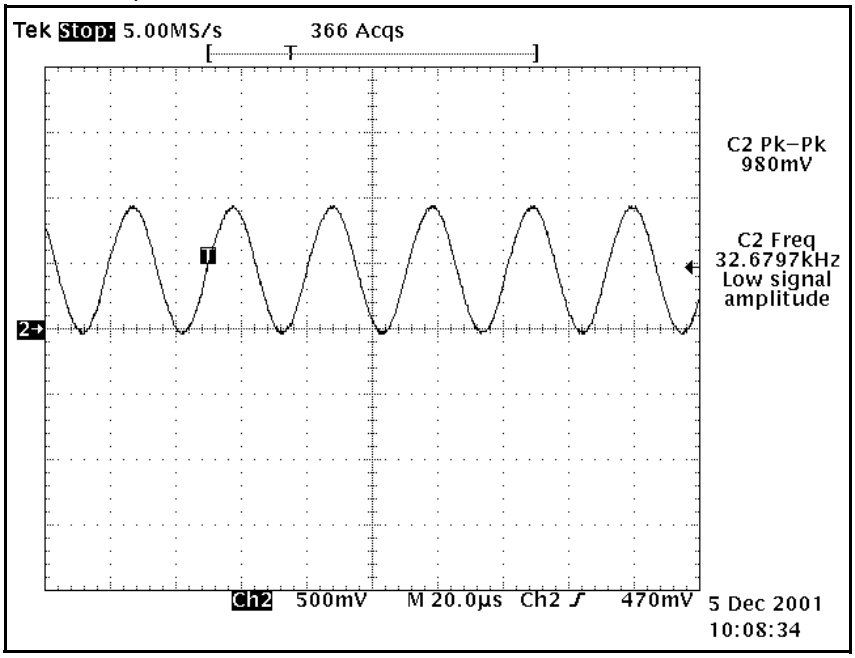


Figure 10: 32 kHz analog waveform at 32 KHz crystal input

Flash Programming Error Codes

The following characteristics apply to the information in Table 3.

- Error codes can be seen from the test results or from Phoenix's flash-tool.
- Underlined information means that the connection under consideration is being used for the first time.

Table 3: Flash Programming Error Codes

Error	Description	Not Working Properly
C101	"The Phone does not set FbusTx line high after the startup."	Vflash1 VBatt BSI and FbusRX from prommer to UEMC. FbusTx from UPP->UEMC->Prommer(SA0)
C102	"The Phone does not set FbusTx line low after the line has been high. The Prommer generates this error also when the Phone is not connected to the Prommer."	PURX(also to Safari) VR3 Rfclock(VCTCXO->Safari->UPP) Mbus from Prommer->UEMC->UPP(MbusRx)(SA0) FbusTx from UPP->UEMC->Prommer(SA1) BSI and FbusRX from prommer to UEMC.
C103	" Boot serial line fail."	Mbus from Prommer->UEMC->UPP(MbusRx)(SA1) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
C104	"MCU ID message sending failed in the Phone."	FbusTx from UPP->UEMC->Prommer
C105	"The Phone has not received Secondary boot codes length bytes correctly."	Mbus from Prommer->UEMC->UPP(MbusRx) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
C106	"The Phone has not received Secondary code bytes correctly."	Mbus from Prommer->UEMC->UPP(MbusRx) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
C107	"The Phone MCU can not start Secondary code correctly."	UPP
C586	"The erasing status response from the Phone informs about fail."	Flash
C686	"The programming status response from the Phone informs about fail."	Flash
Cx81	"The Prommer has detected a checksum error in the message, which it has received from the Phone."	FbusTx from UPP->UEMC->Prommer
Cx82	"The Prommer has detected a wrong ID byte in the message, which it has received from the Phone."	FbusTx from UPP->UEMC->Prommer

Table 3: Flash Programming Error Codes (Continued)

Error	Description	Not Working Properly
A204 Cx83 Cx84 Cx85	"The flash manufacturer and device IDs in the existing algorithm files do not match with the IDs received from the target phone." "The Prommer has not received phone acknowledge to the message." "The phone has generated NAK signal during data block transfer." "Data block handling timeout"	Flash UPP VIO/VANA Signals between UPP-Flash Mbus from Prommer->UEMC->UPP(MbusRx) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
Cx87	"Wrong MCU ID."	RFClock UPP(Vcore)
Startup for flashing	Required startup for flashing	Vflash1 VBatt

Charging Operation

Battery

The 2118 uses a Lithium-Ion cell battery with a capacity of 850 mAh. Reading a resistor inside the battery pack on the BSI line indicates the battery size. The mobile terminal measures the approximate temperature of the battery on the BTEMP line with an NTC resistor on the PCB.

The temperature and capacity information are needed for charge control. These resistors are connected to the BSI pin of the battery connector and the BTEMP of the mobile terminal. The mobile terminal has 100 kΩ pull-up resistors for this line so that they can be read by A/D inputs in the mobile terminal.

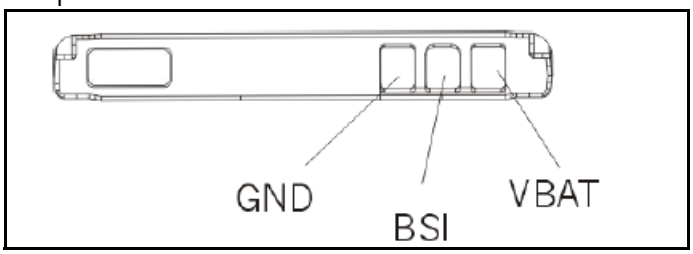


Figure 11: BL-5C battery pack pin order

Charging Circuitry

The UEMC ASIC controls charging depending on the charger being used and the battery size. External components are needed for EMC, reverse polarity, and transient protection of the input to the baseband module. The charger connection is through the system connector interface. The baseband is designed to support DCT3 chargers from an electrical point of view. Both 2- and 3-wire type chargers are supported. However, the 3-wire chargers are treated as a 2-wire charger.

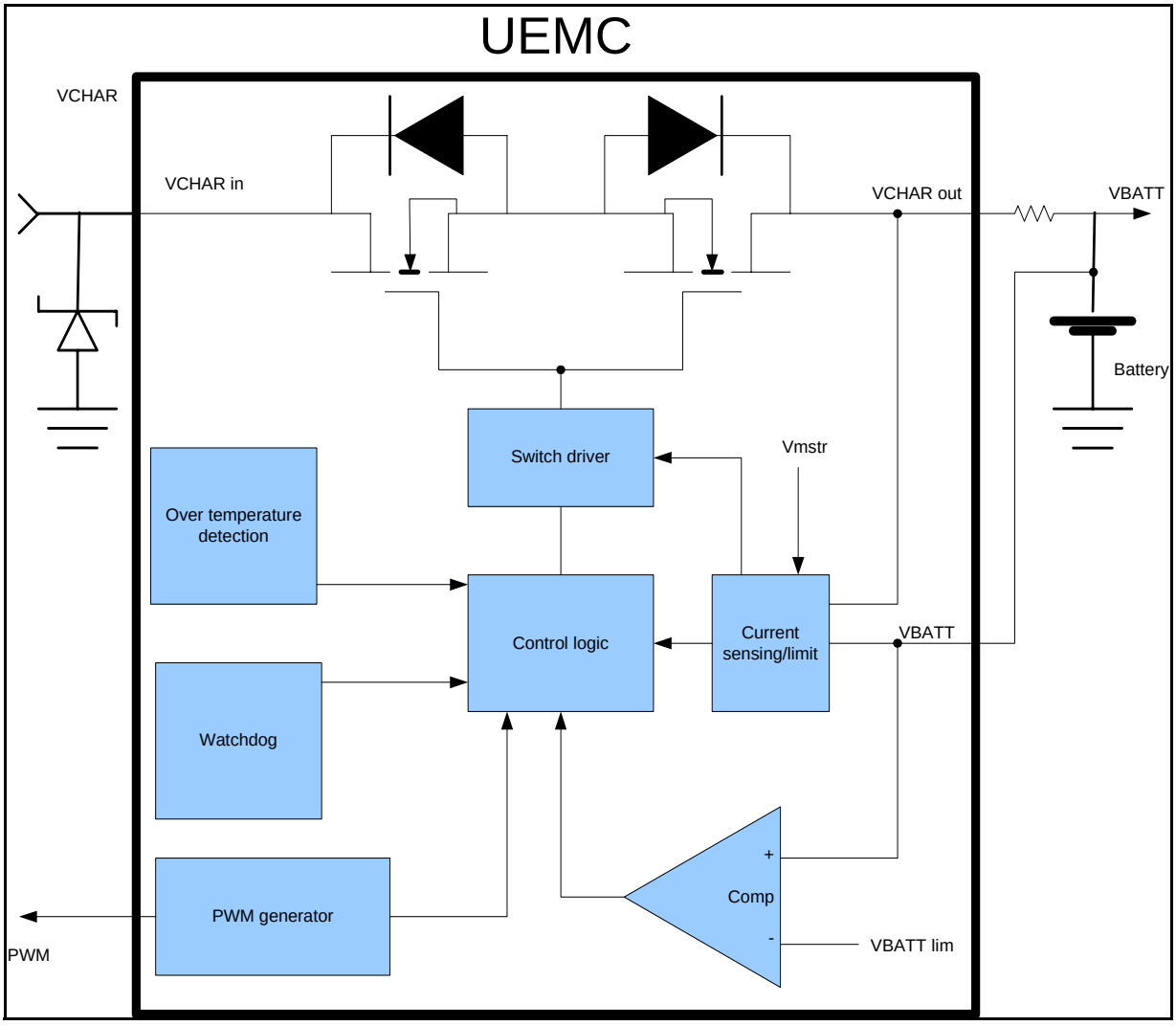


Figure 12: Charging circuitry

Charger Detection

Connecting a charger creates voltage on the VCHAR input of the UEMC. Charging starts when the UEMC detects the VCHAR input voltage level above 2 V (VCHdet+ threshold). The VCHARDET signal is generated to indicate the presence of the charger for the SW. The EM SW controls the charger identification/acceptance. The charger recognition is initiated when the EM software receives a "charger connected" interrupt. The algorithm basically consists of the following three steps:

1. Check that the charger output (voltage and current) is within safety limits.
2. Identify the charger as a 2-wire or 3-wire charger.
3. Check that the charger is within the charger window (voltage and current).

If the charger is accepted and identified, the appropriate charging algorithm is initiated.

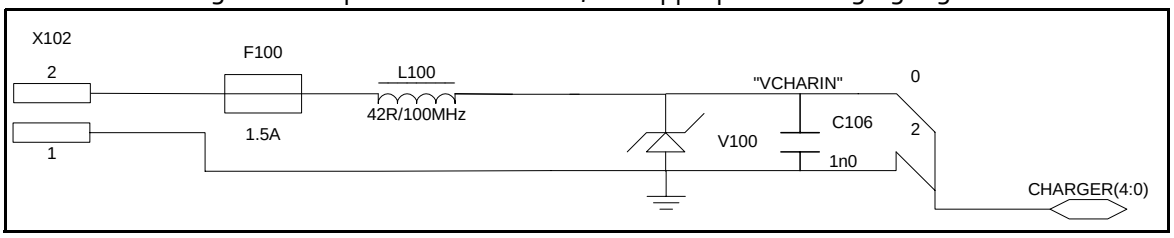


Figure 13: Charging circuit

Charge Control

In active mode, charging is controlled by the UEMC's digital part. Charging voltage and current monitoring is used to limit charging into safe area. For this reason, the UEMC has the following programmable charge cut-off limits:

- VBATLim1=3.6 V (Default)
- VBATLim2L=5.0 V
- VBATLim2H=5.25 V

VBATLim1, 2L, 2H are designed with hystereses. When the voltage rises above VBATLim1, 2L, 2H+ charging is stopped by turning the charging switch off. No change is done in operational mode. After the voltage has decreased below VBATLim-, charging restarts.

There are two PWM frequencies in use depending on the type of the charger. A 2-wire charger uses a 1 Hz, while a 3-wire charger uses a 32Hz. The duty cycle range is 0% to 100%. The maximum charging current is limited to 1.2 A.

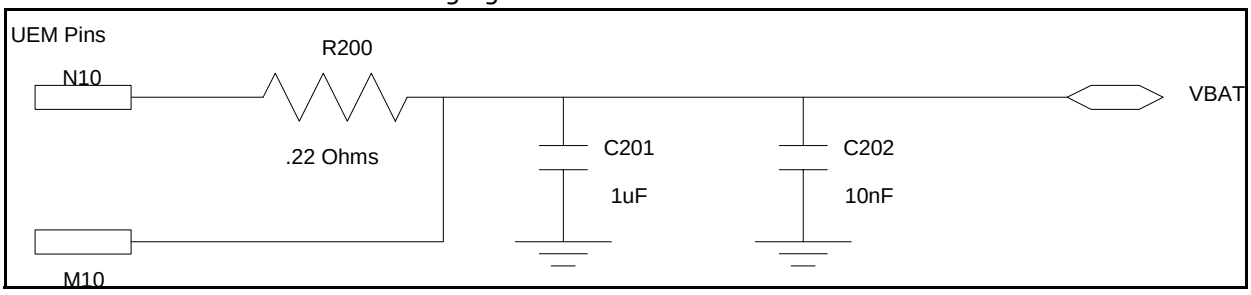


Figure 14: Charging circuity at the battery

Audio

The audio control and processing is provided by UEMC, which contains the audio codec, and the UPP, which contains the MCU and DSP blocks. These blocks handle and process the audio data signals.

The baseband supports three microphone inputs and two earpiece outputs. The microphone inputs are MIC1, MIC2, and MIC3. MIC1 input is used for the mobile terminal's internal microphone; MIC2 input is used for headsets (HDB-4). MIC3 is not used. Every microphone input can have either a differential or single-ended AC connection to UEMC circuit. The internal microphone (MIC1) and external microphone (MIC2) for Pop-port^{TM} accessory detection are both differential. The microphone signals from different sources are connected to separate inputs at UEMC. Inputs for the

microphone signals are differential types. Also, MICBIAS1 is used for MIC1 and MICBIAS2 is used for MIC2. The 2118 also supports a hands-free speaker (B301), which is driven by an IHF audio amplifier (N150).

Display and Keyboard

The 2118 uses LEDs for LCD and keypad illumination. There is one LED for the LCD and four LEDs for the keypad. KLIGHT is the signal used to drive the LED driver for the LCD and keyboard. This signal turns on the LED driver (N302).

The 2118 also uses an IOS LCD. The interface uses a 9-bit data transfer and is quite similar to the DCT3 type interface, except the Command/Data information is transferred together with the data.

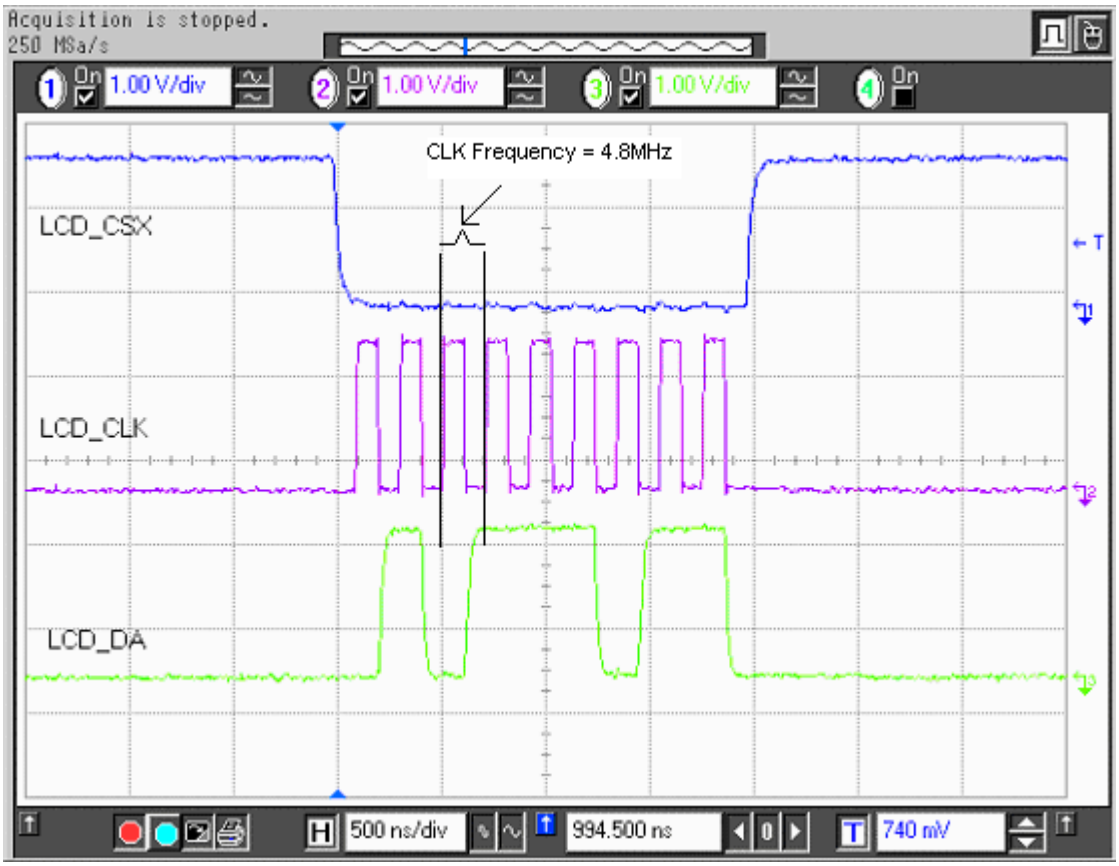


Figure 15: Waveform for the LCD Interface

Flashlight

The flashlight is driven by the white LED driver and controlled by the UEMC. The TK65600B-G is an active-high enable device, which is tied to the DLIGHT signal from the UEMC.

Accessories

The 2118 supports Pop-port and Universal Headset accessories, differential and single-ended, respectively. Detection of the Pop-port accessories is done through the ACI signal where the Universal Headset is detected on GenIO (12).

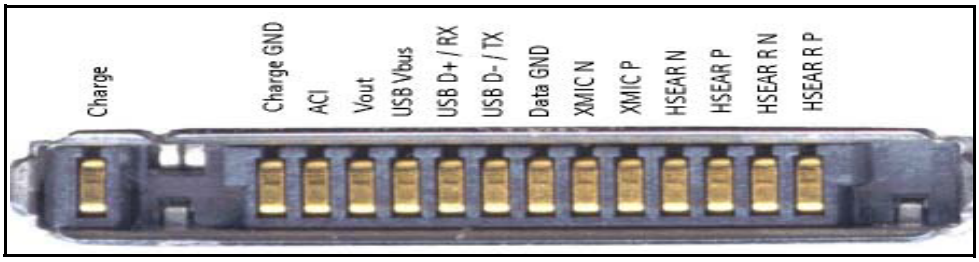


Figure 16: Pop-port connector pin out

The pin out on the Pop-port connector is as follows:

- Charger
- Charger GND
- ACI
- Vout
- USB Vbus
- USB D+ / Fbus Rx
- USB D- / Fbus Tx
- Data GND
- XMic N
- XMic P
- HSear N
- HSear P
- HSear R N
- HSear R P

You can perform the following in Pop-port accessories:

- Charging
- Accessory detection
- FBUS communication
- Fully differential audio interface for mono- and stereo outputs

Charging

Charging through Pop-port is accomplished in the same manner as through the charger connector. Pin 1 of the Pop-port is physically connected to the charger connector. When the mobile terminal is connected to a desktop charger (e.g., DCV-15), it charges in the same manner as it does with the charger connector.

Figure 17 shows the actual charging sequence. The channels on the diagram are:

- CH1 = Charging current across the .22 Ohm (R200) resistor on UEMK
- CH2 = Charger voltage measure at V100
- CH3 = Battery voltage measure at R200
- CH4 = PURX

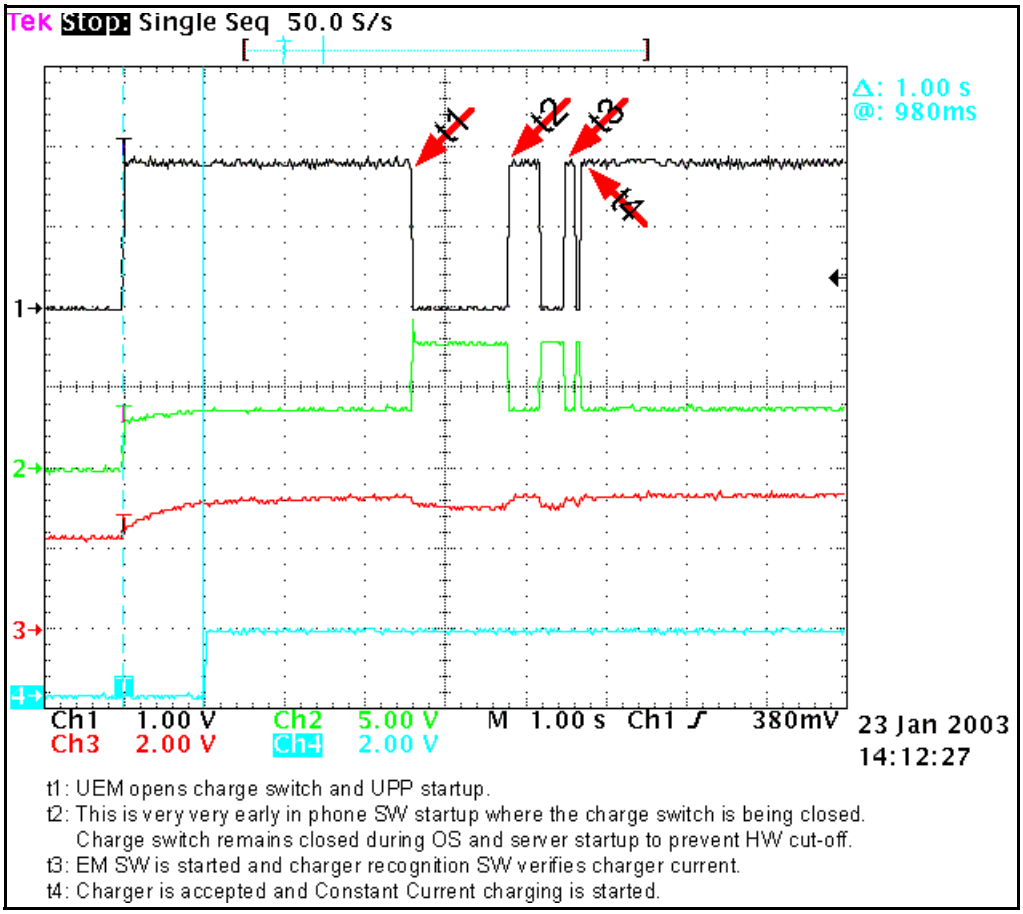


Figure 17: Charging sequence

In Channel 4, PURX is released, which this indicates when the mobile terminal operation goes from RESET mode to POWER_ON mode.

Pop-port Headset Detection

Accessory detection on the Pop-port is done digitally. The pins used for this accessory detection are:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout)

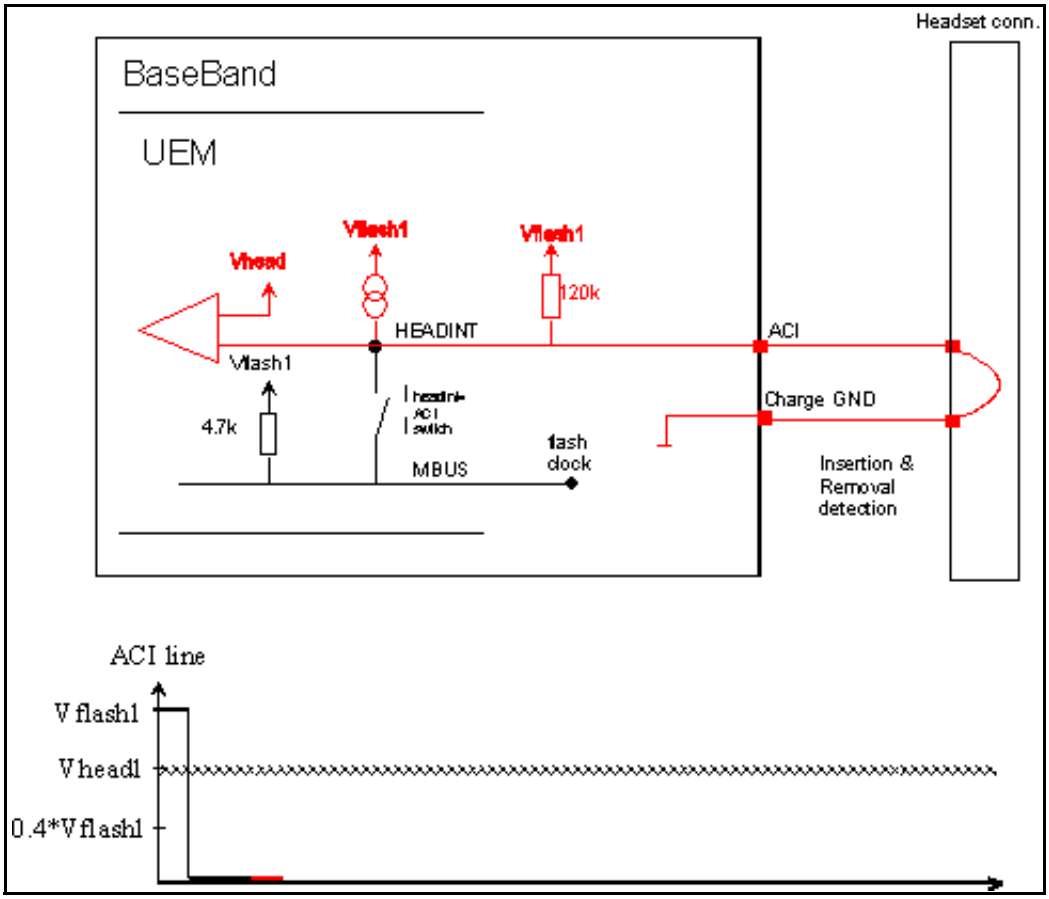


Figure 18: Waveform showing Pop-port accessory detection

FBus Detection

FBus communication in Pop-port is done through the following lines:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout)
- Pin 6 (FBus Rx)
- Pin 7 (FBus Tx)

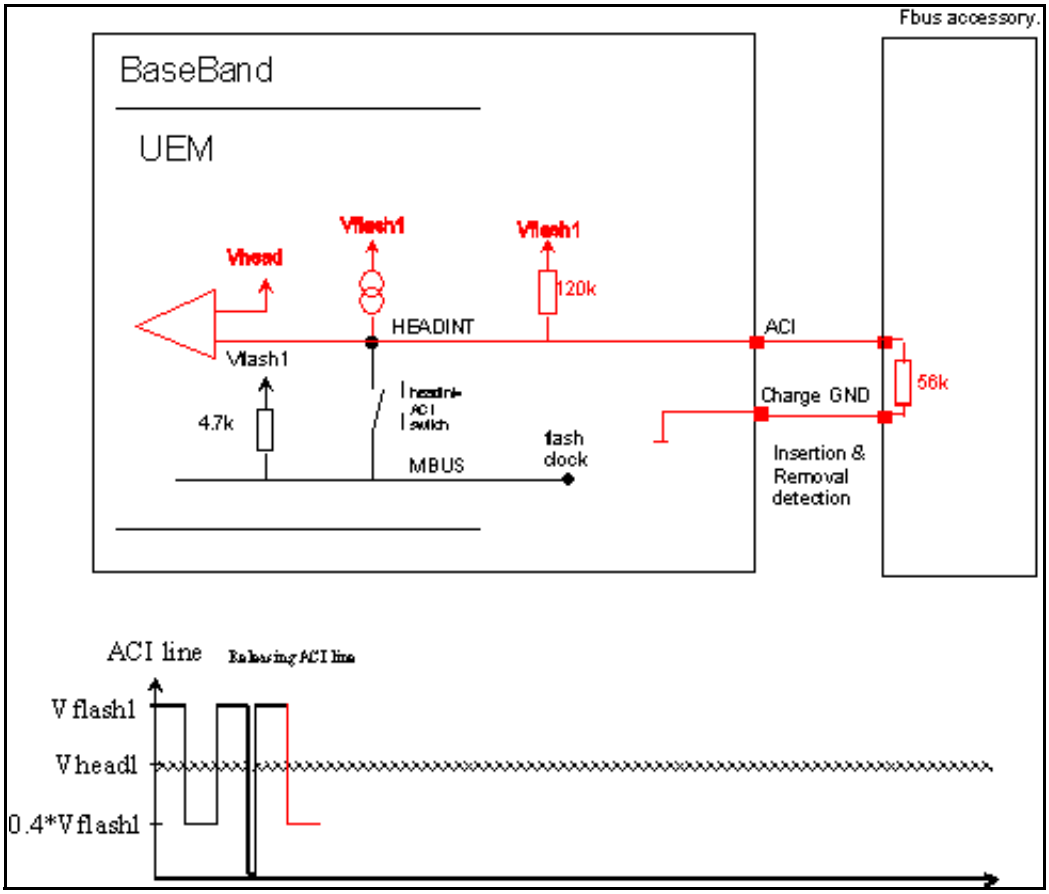


Figure 19: Waveform showing Pop-port FBus communication

Accessory Detection Through ACI

USB and Audio on (mono or stereo)/FM radio communication in Pop-port is done through the following signals:

Table 4: Accessory Detection Signals

USB	Audio/FM
Pin 5 (USB Vbus)	Pin 9 (XMic N)
Pin 6 (USB +)	Pin 10 (SMIC P)
Pin 7 (USB -)	Pin 11 (HSEAR N)
Pin 8 (Data GND)	Pin 12 (HSEAR P)
	Pin 13 (HSEAR R N)
	Pin 14 (HSEAR R P)

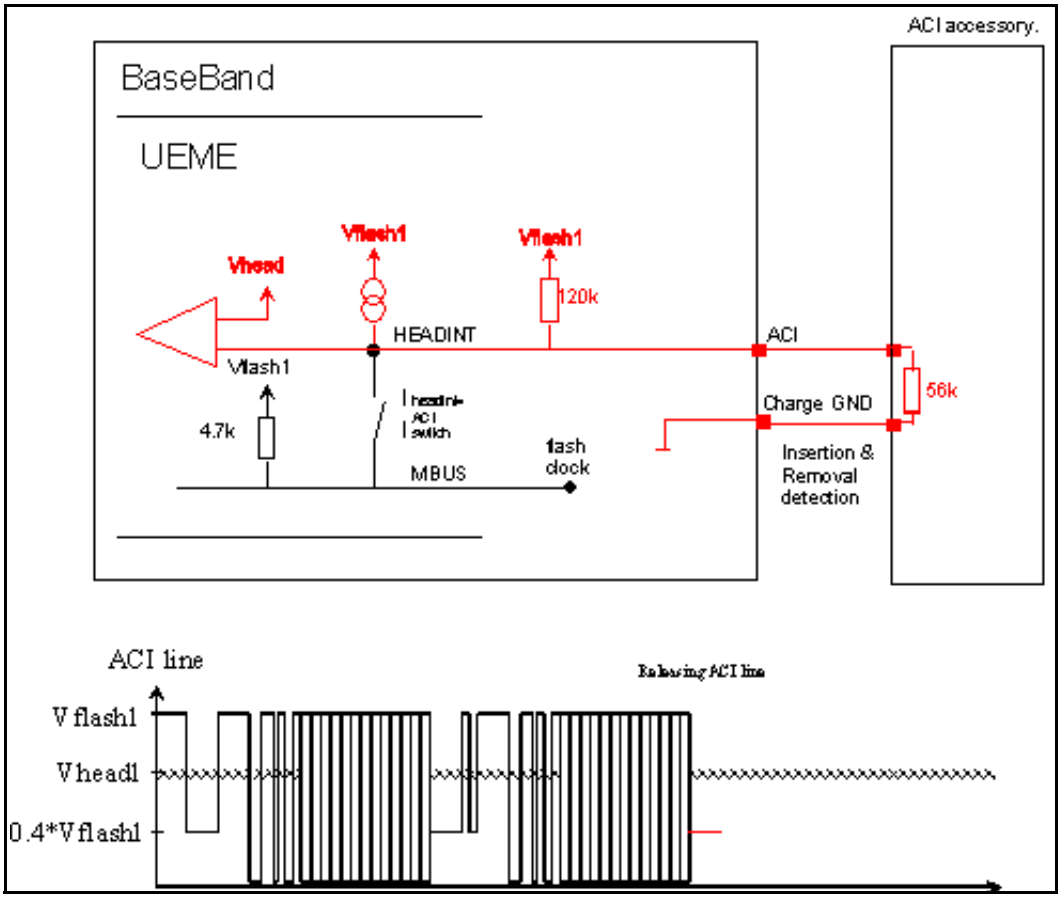


Figure 20: Waveform showing accessory detection through ACI

SIM CAR

The 2118 supports SIM CAR. Use the waveform in Figure 21 to verify that the sim_vcc, sim_i/o, cim_clk, and sim_rst signals are activated in the correct sequence at power up. This picture may be taken when the SIM CAR is installed on the mobile terminal to measure the signals when the mobile terminal is turned on. The figure shows the proper waveforms when the interface is working. See Figure 23 on page 29 for the test point's location.

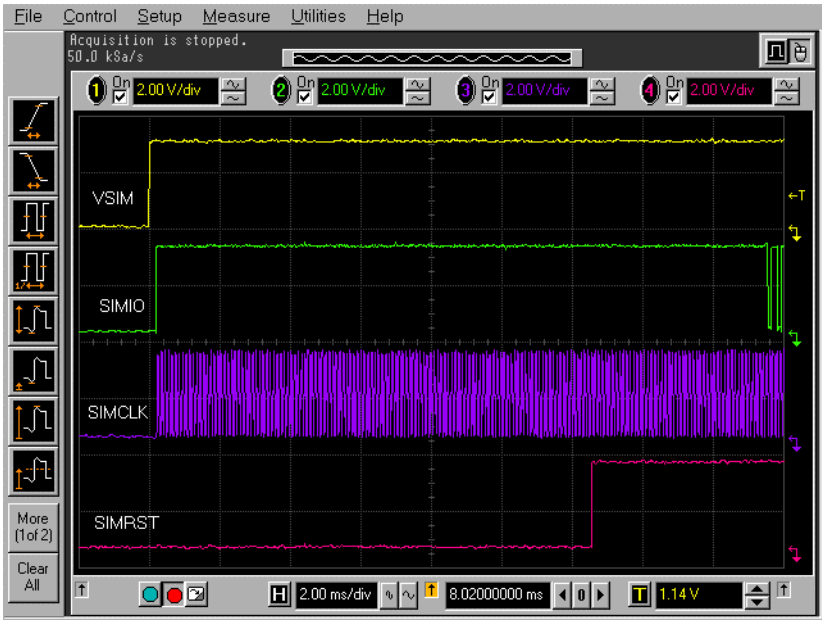


Figure 21: RUIM signal waveform

Test Points

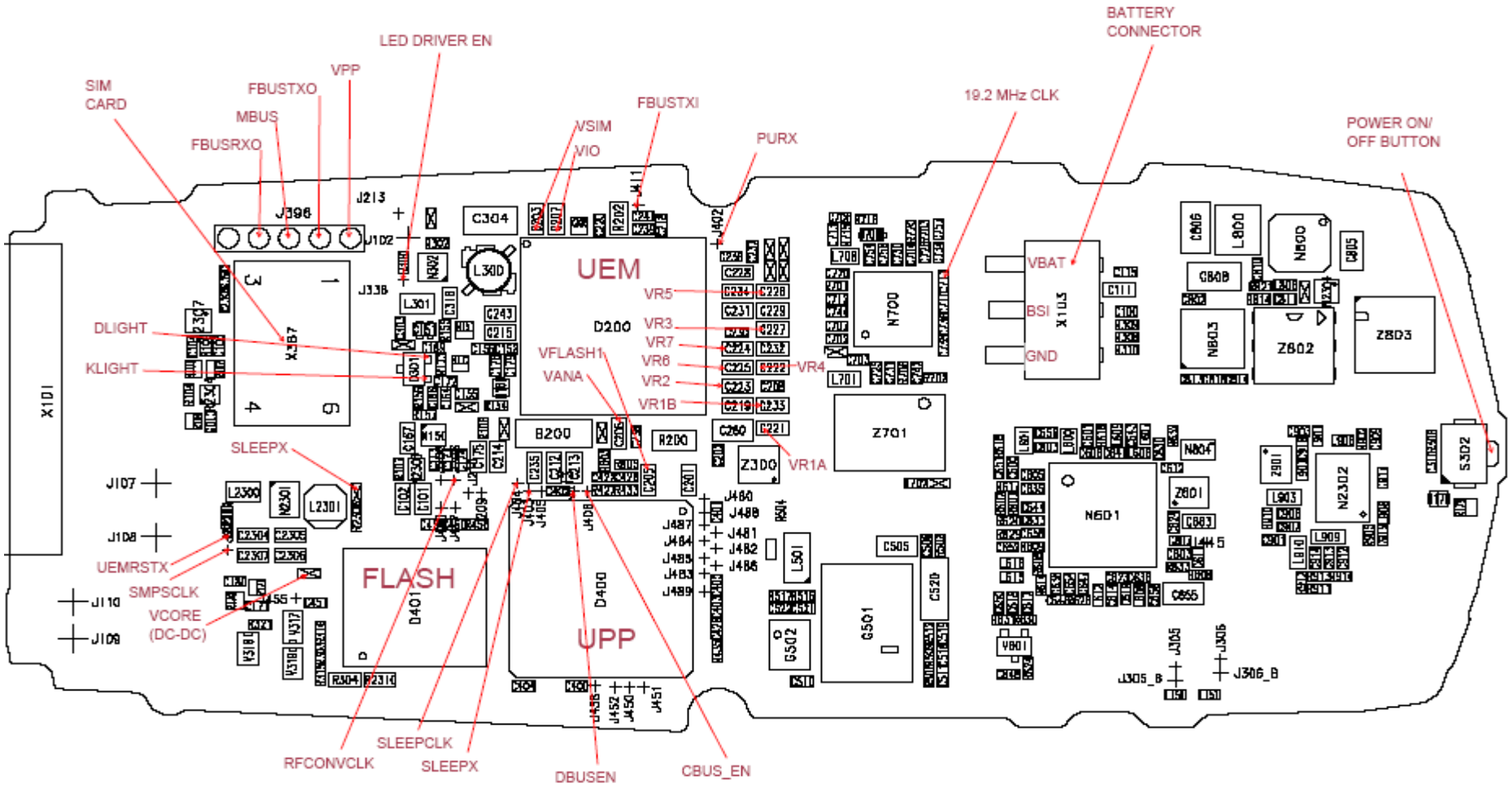


Figure 22: Test points (bottom)

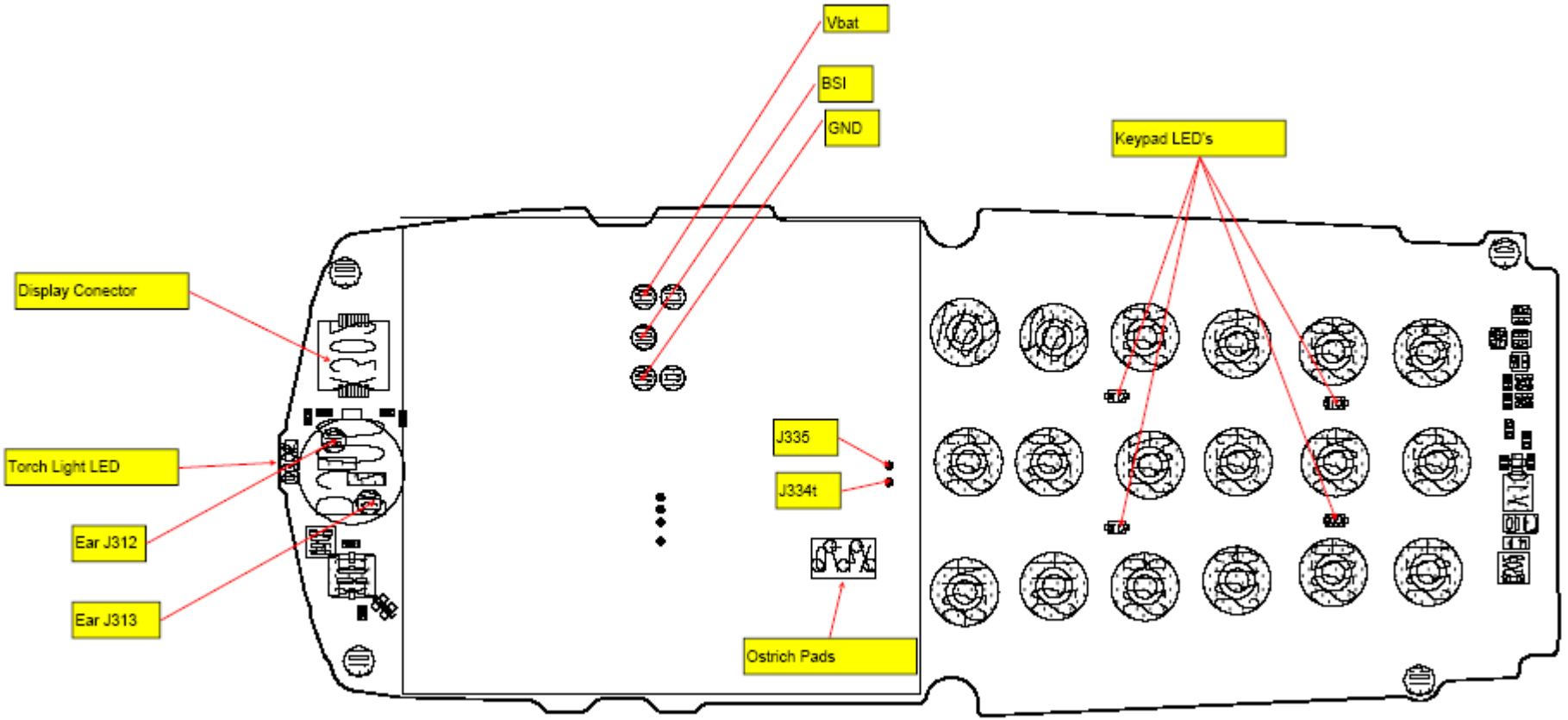


Figure 23: BB test points (top)

Troubleshooting

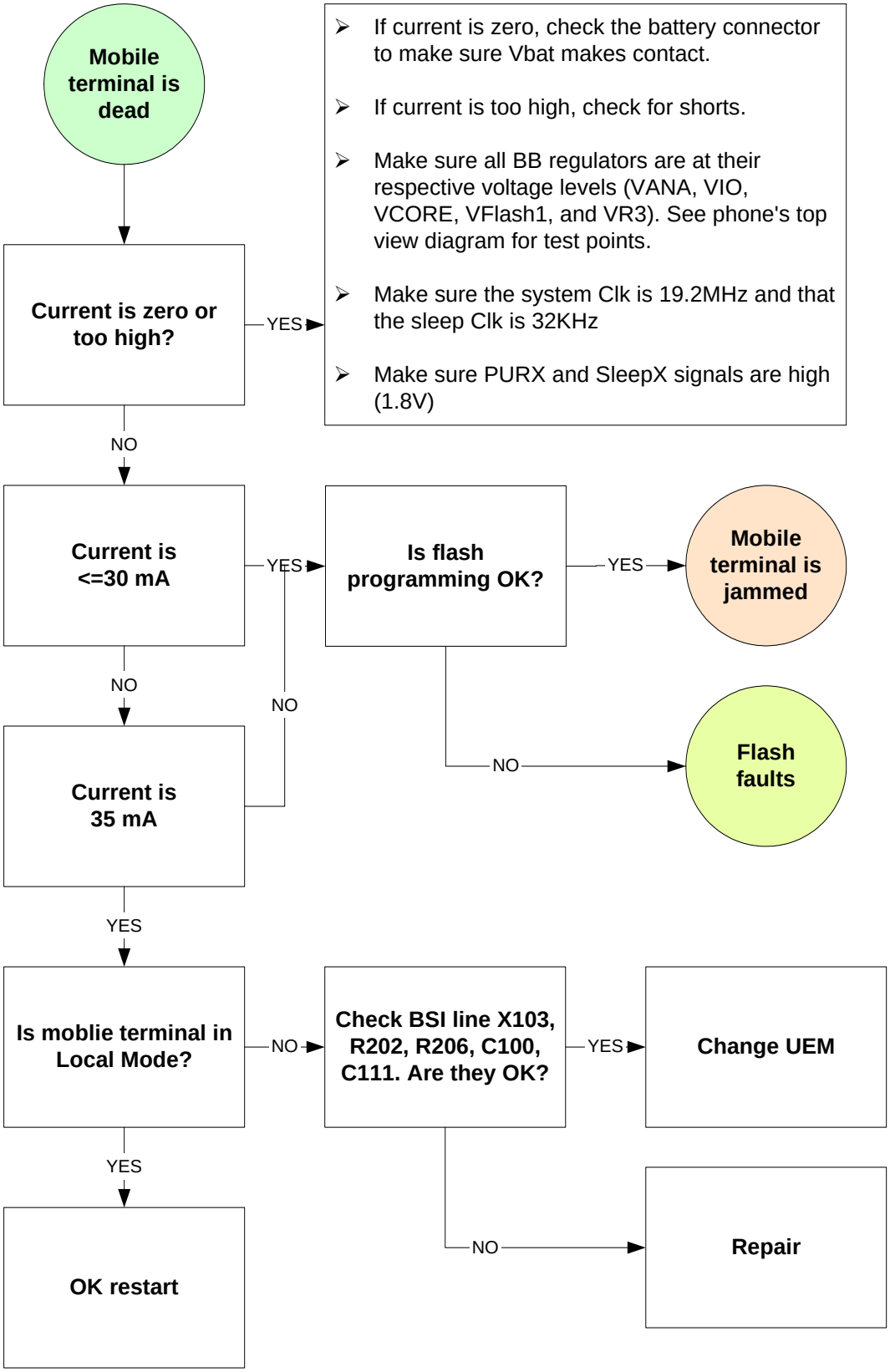
The following hints should help finding the cause of the problem when the circuitry seems to be faulty. Troubleshooting instructions are divided into the following sections:

- Mobile terminal is totally dead
- Power does not stay on or the mobile terminal is jammed
- Flash programming does not work
- Display is not working
- Audio fault
- Charging fault

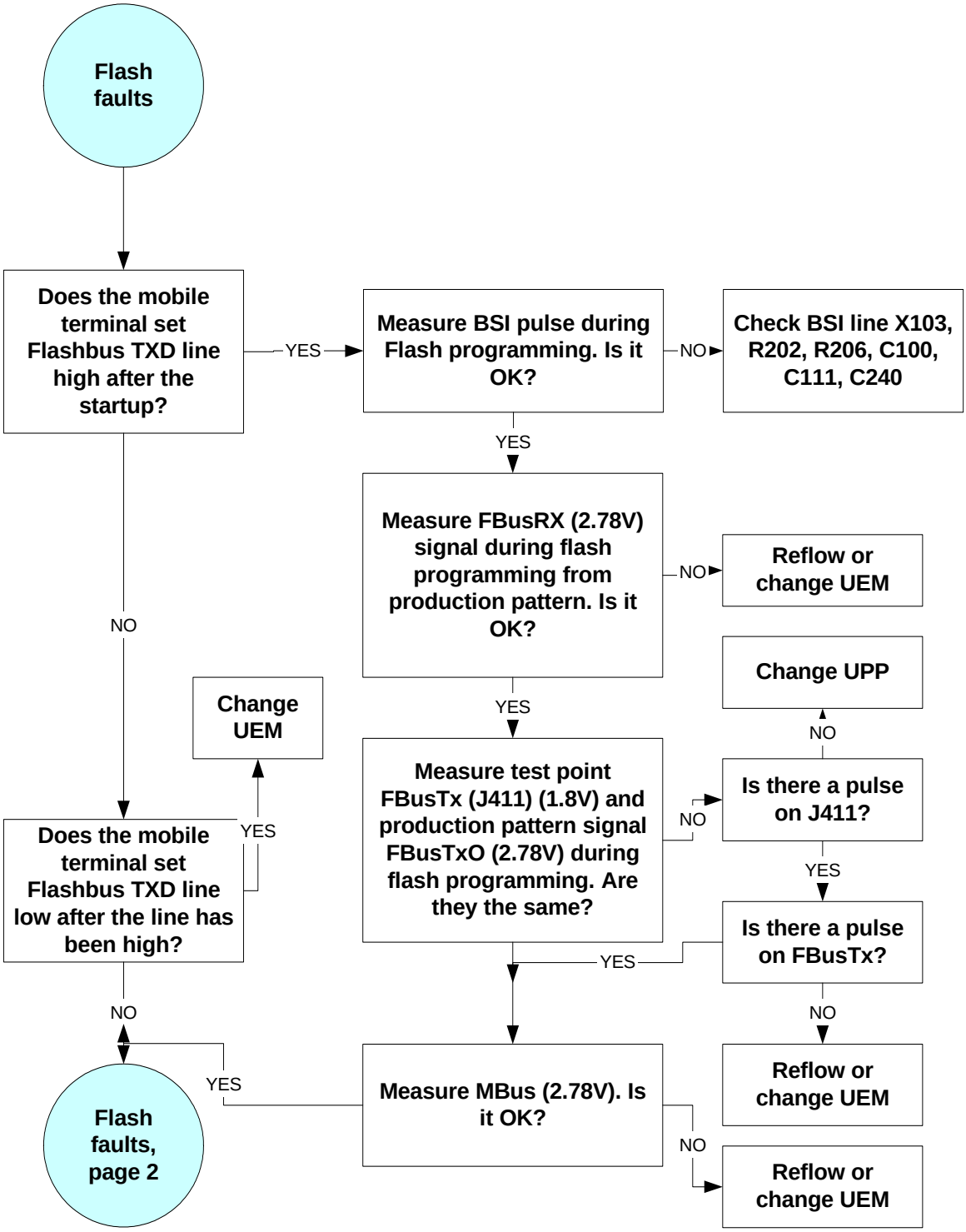
First, carry out a through visual check of the module. Ensure in particular that:

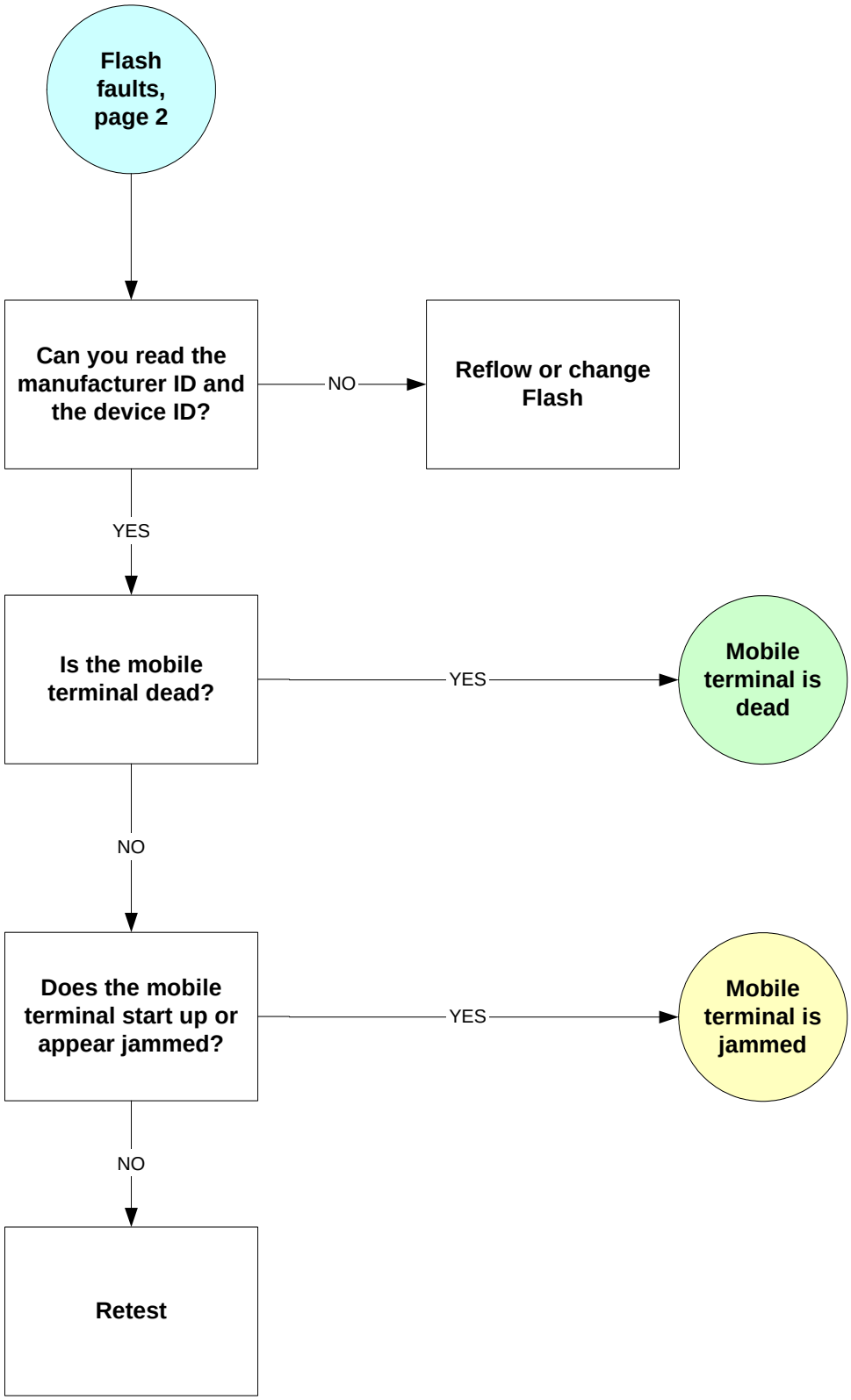
- There are no mechanical damages
- Soldered joints are okay
- ASIC orientations are okay

Mobile Terminal is Dead

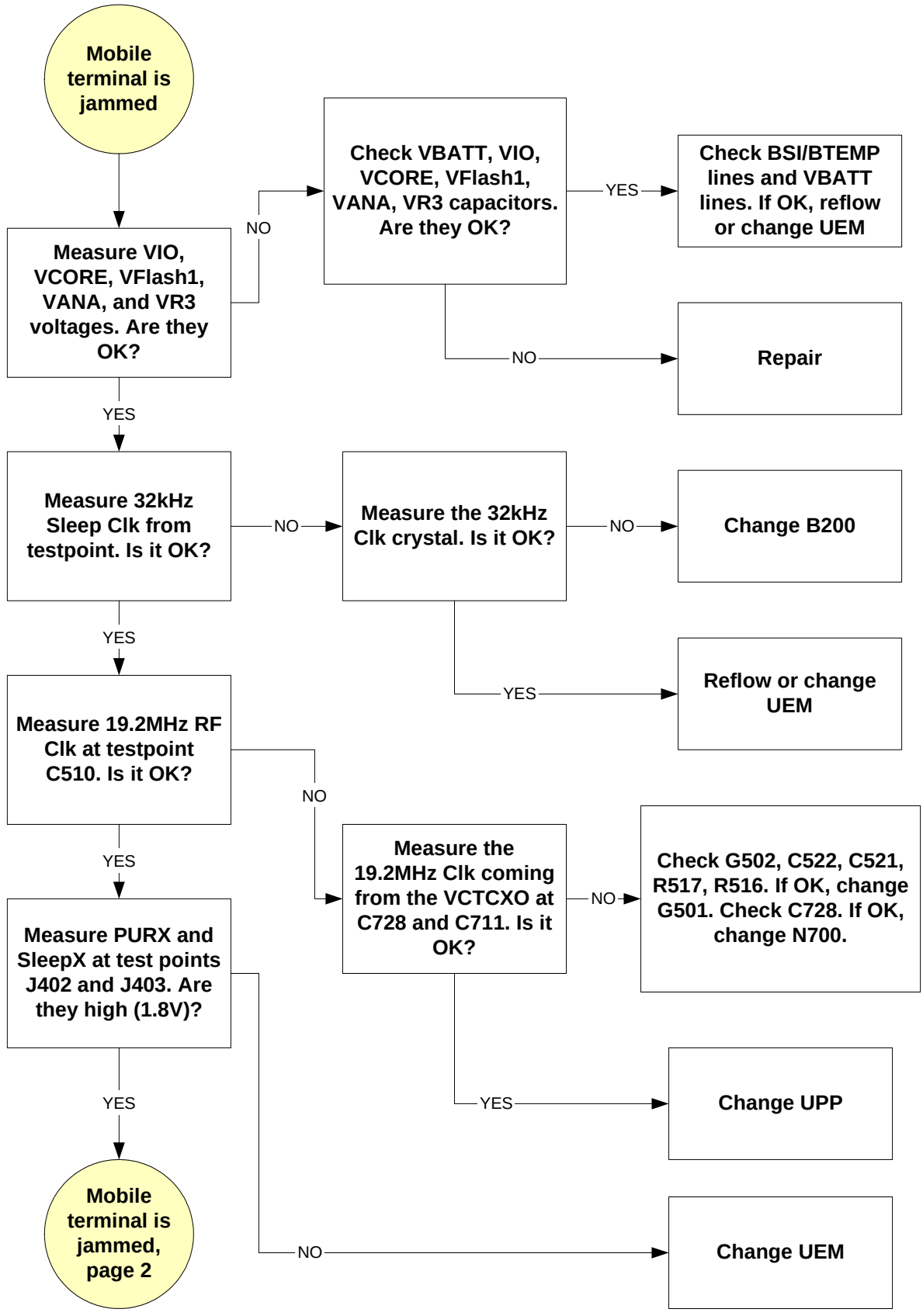


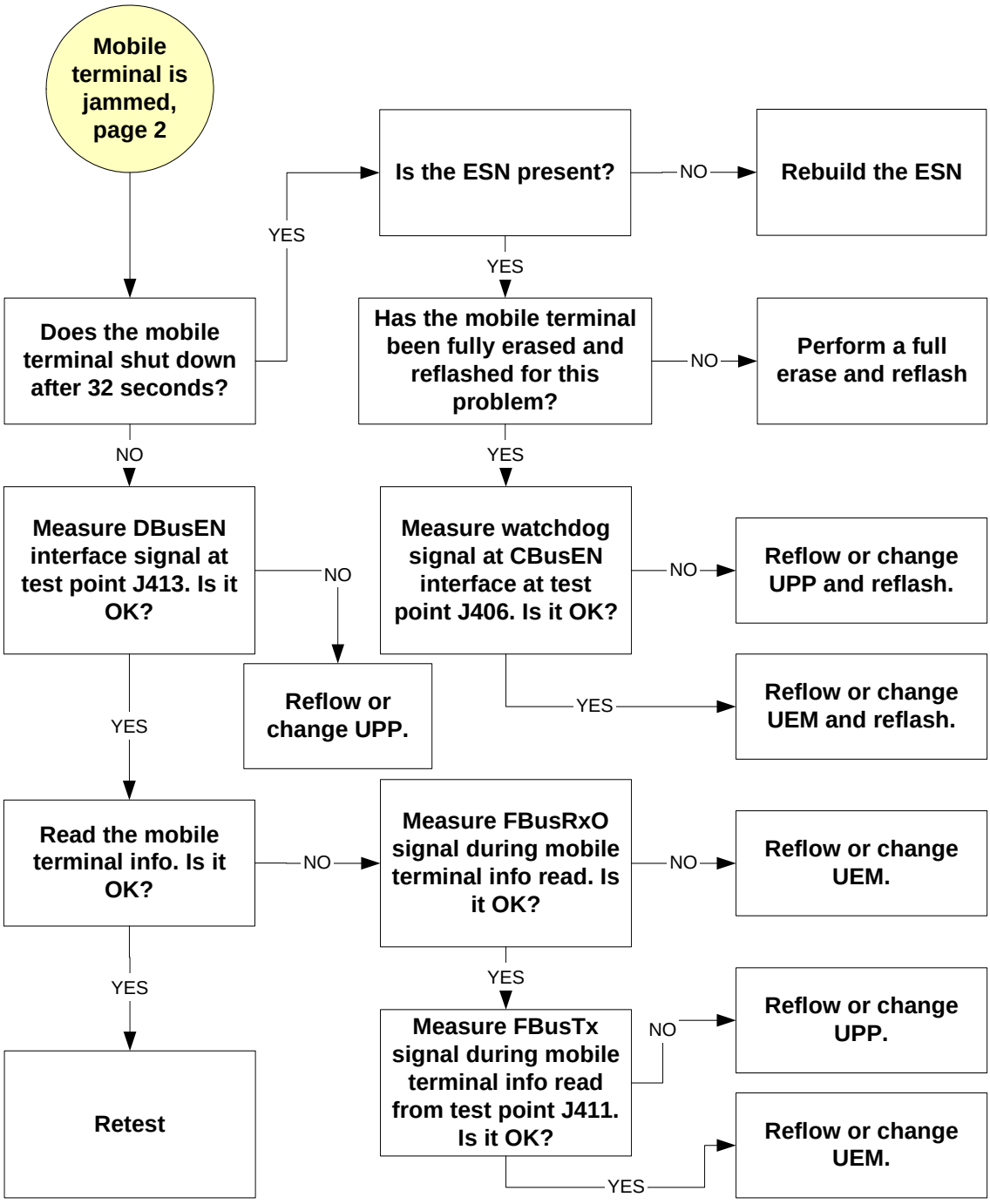
Flash Programming Does Not Work



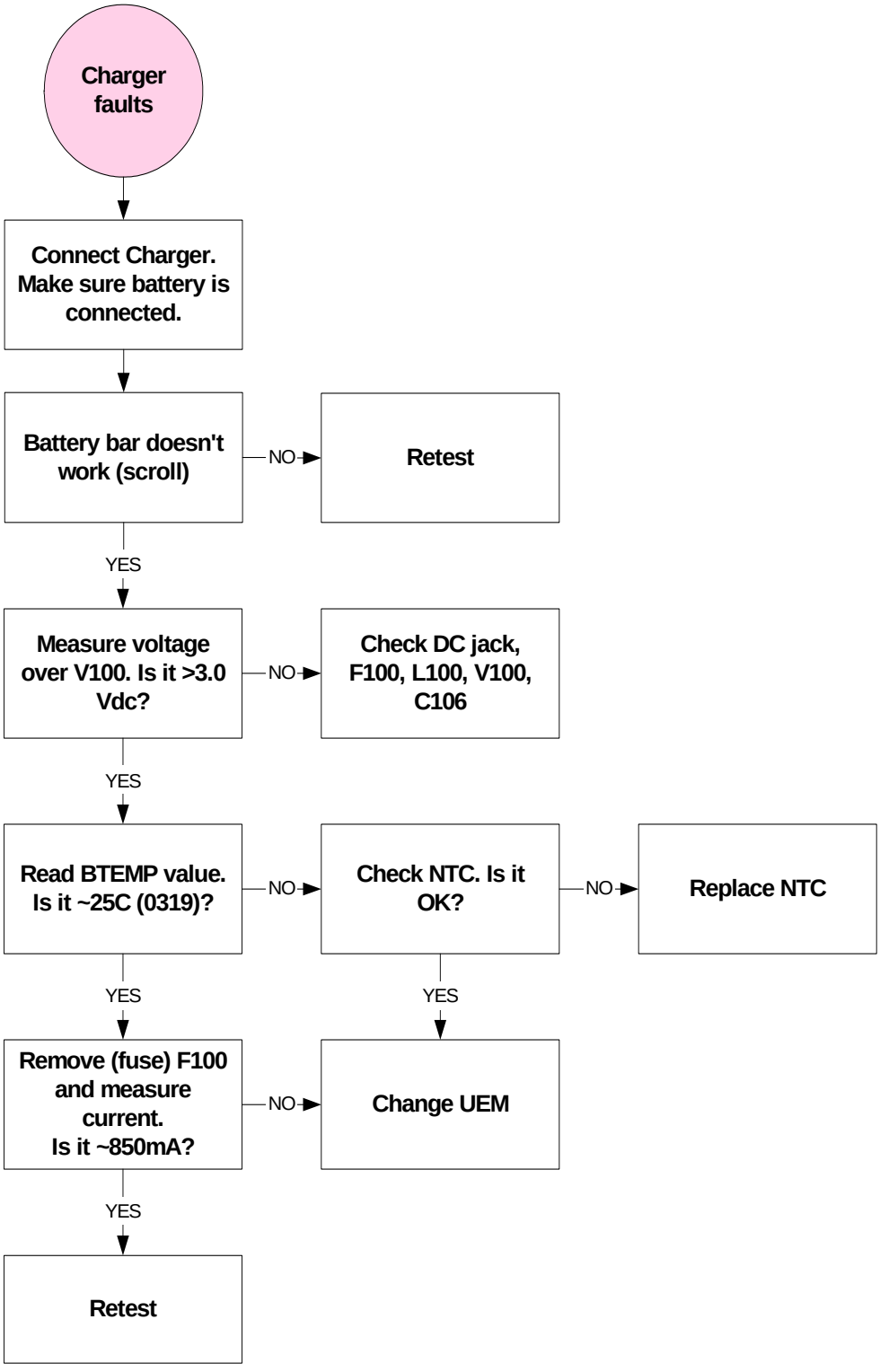

Flash faults, page 2
Can you read the manufacturer ID and the device ID?
NO
Reflow or change Flash
YES
Is the mobile terminal dead?
YES
Mobile terminal is dead
NO
Does the mobile terminal start up or appear jammed?
YES
Mobile terminal is jammed
NO
Retest

Power Does Not Stay on or the Mobile Terminal is Jammed

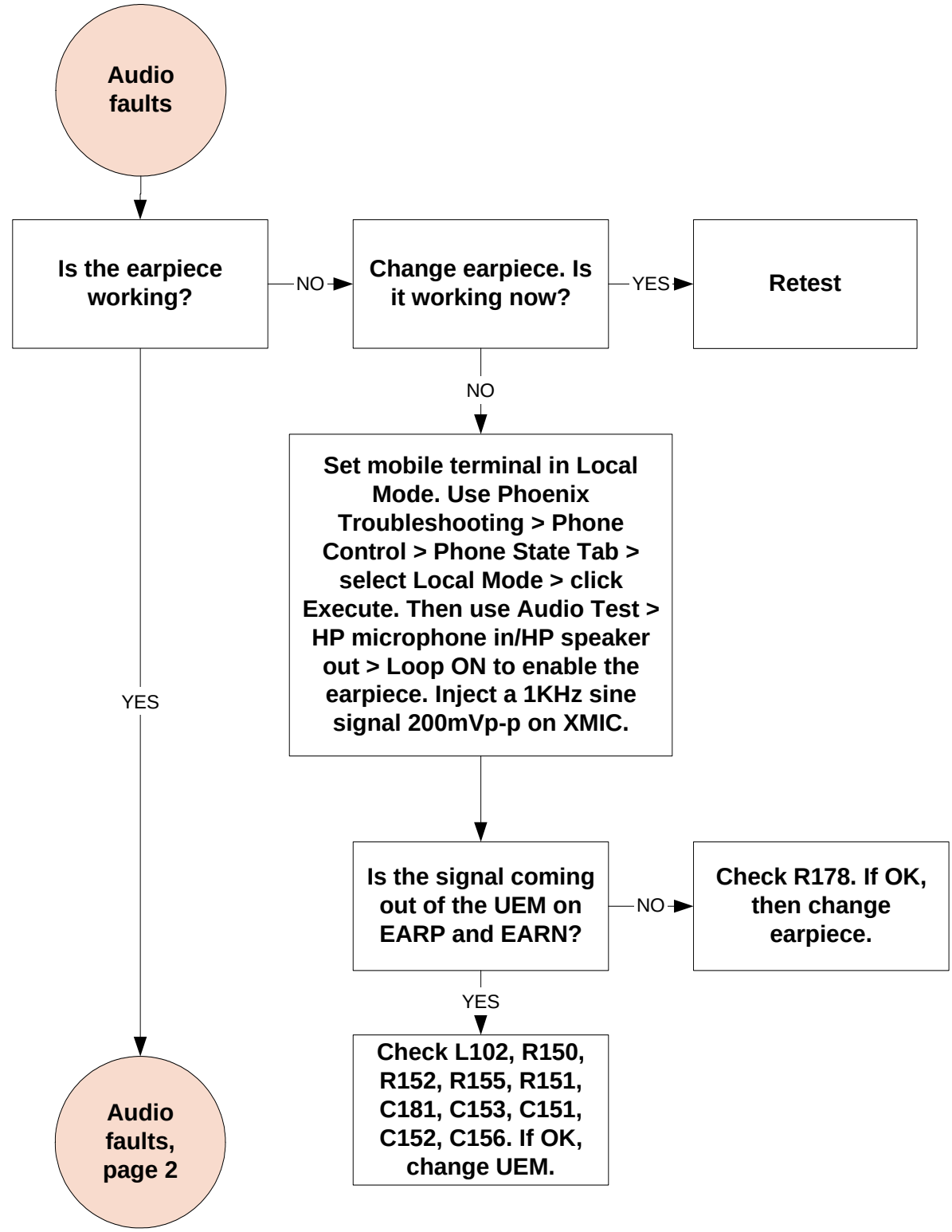


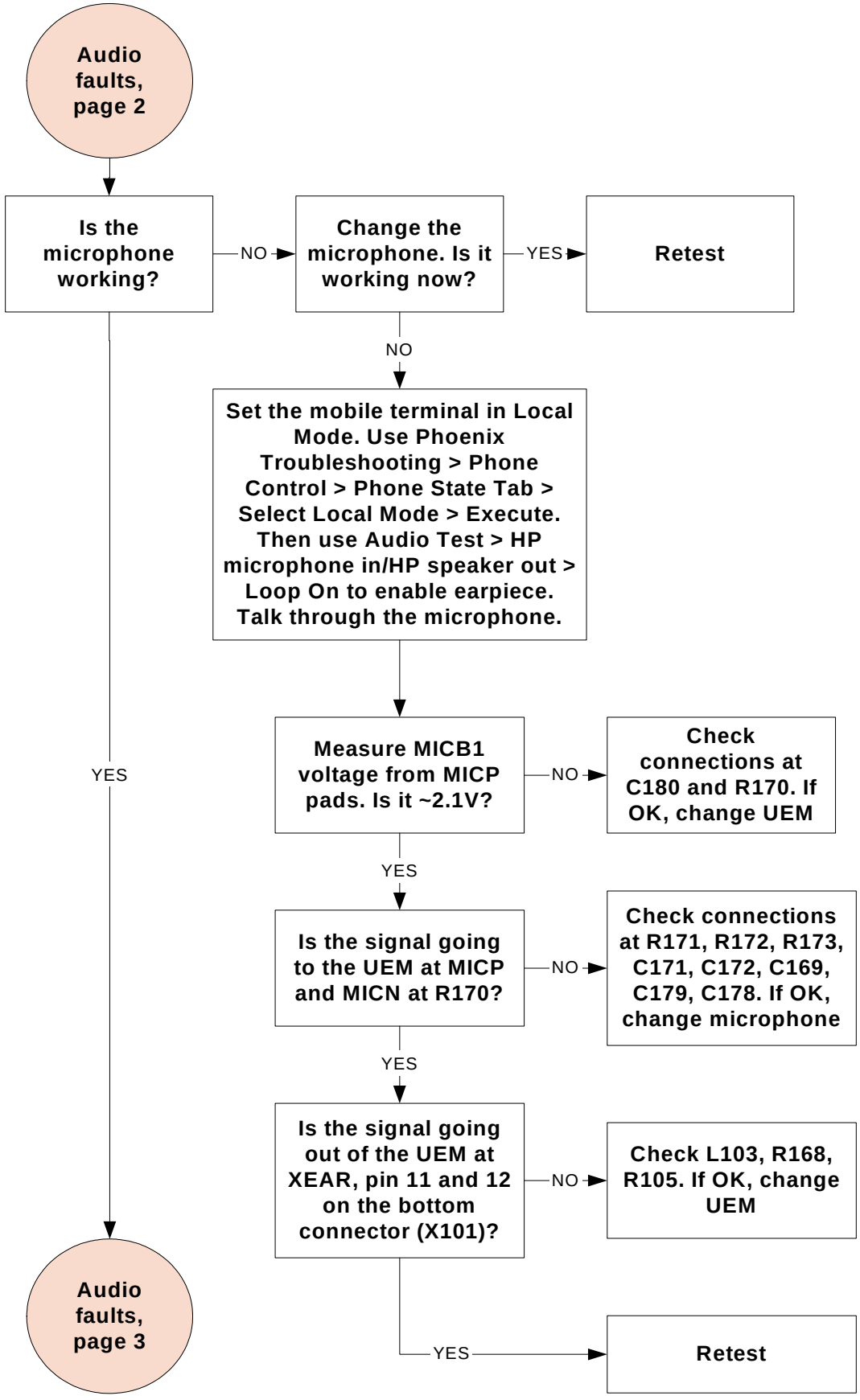

Mobile terminal is jammed, page 2
Is the ESN present?
NO
Rebuild the ESN
YES
YES
Does the mobile terminal shut down after 32 seconds?
Has the mobile terminal been fully erased and reflashed for this problem?
NO
Perform a full erase and reflash
NO
YES
Measure DBusEN interface signal at test point J413. Is it OK?
Measure watchdog signal at CBusEN interface at test point J406. Is it OK?
NO
Reflow or change UPP and reflash.
NO
Reflow or change UPP.
YES
Reflow or change UEM and reflash.
YES
Read the mobile terminal info. Is it OK?
Measure FBusRxO signal during mobile terminal info read. Is it OK?
NO
Reflow or change UEM.
NO
YES
YES
Measure FBusTx signal during mobile terminal info read from test point J411. Is it OK?
NO
Reflow or change UPP.
Retest
Reflow or change UEM.
YES

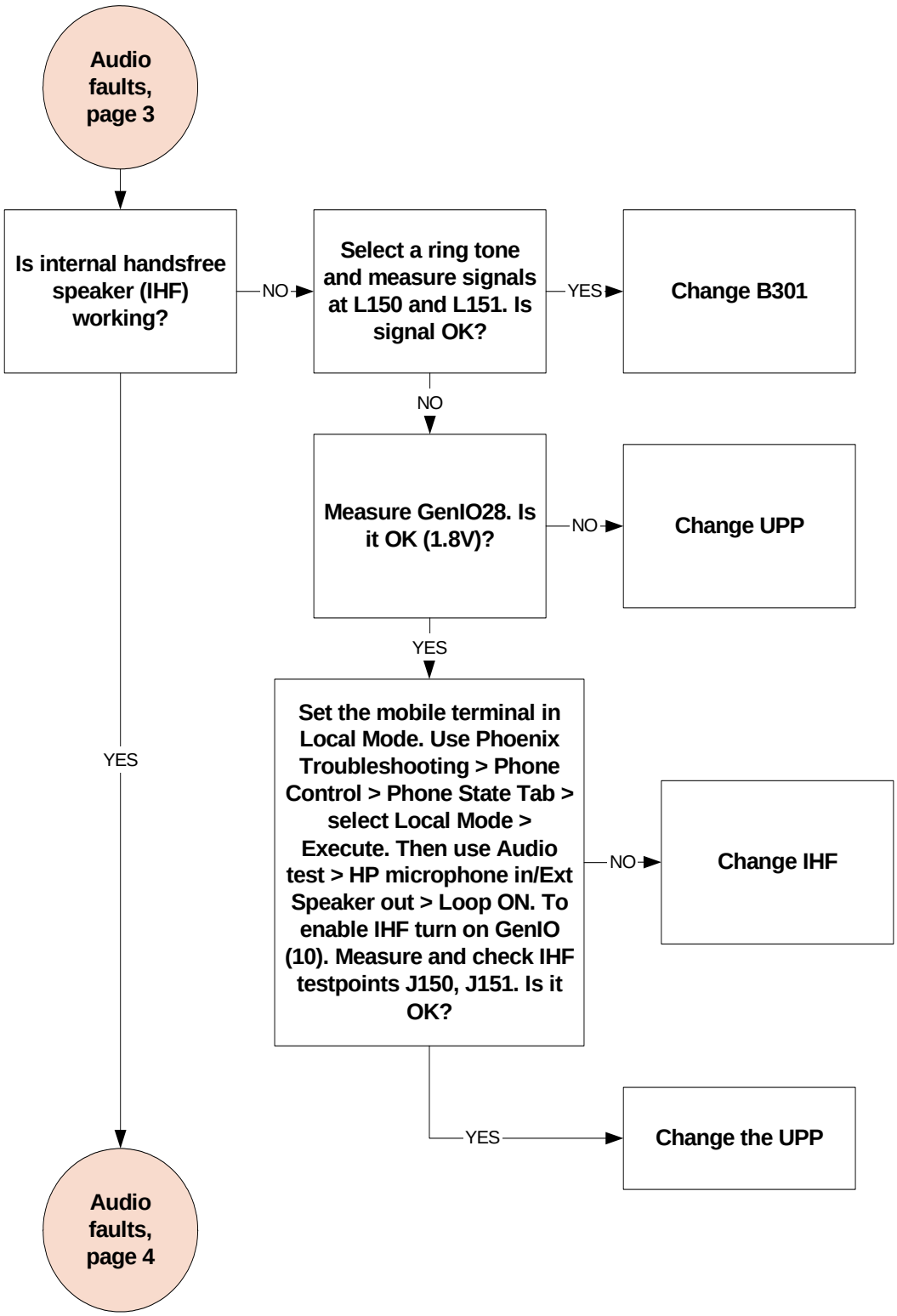
Charger

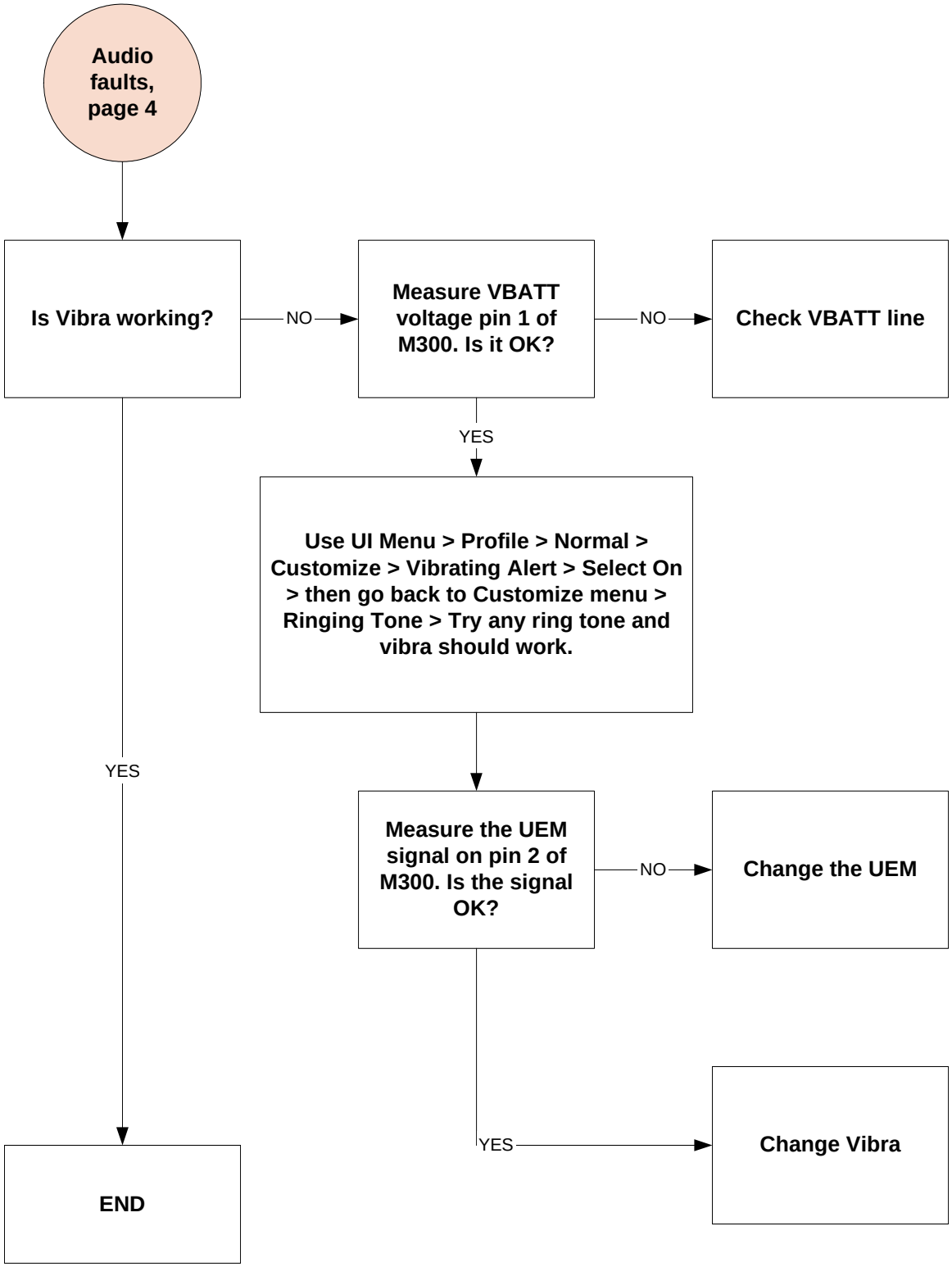


Audio Faults

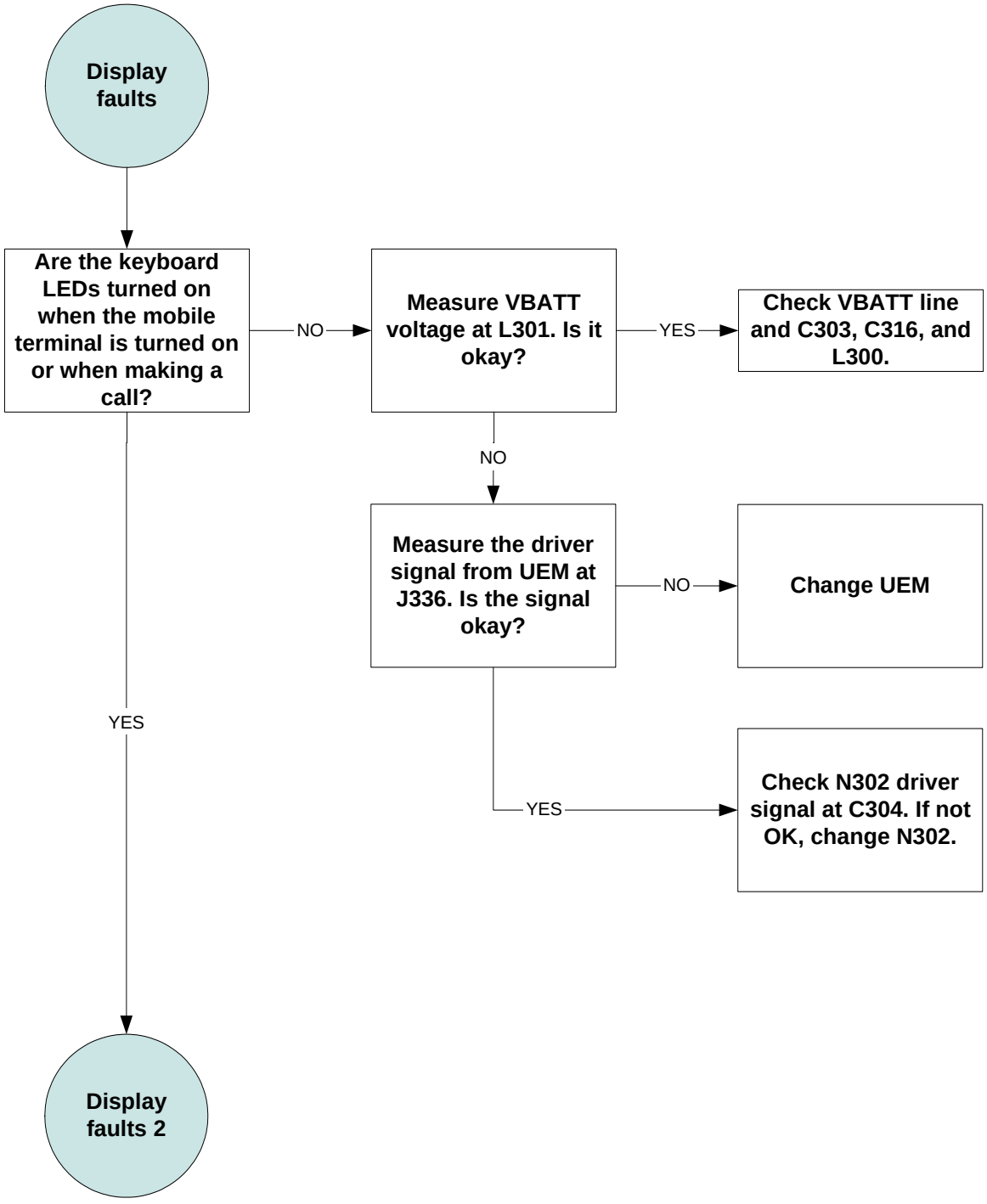


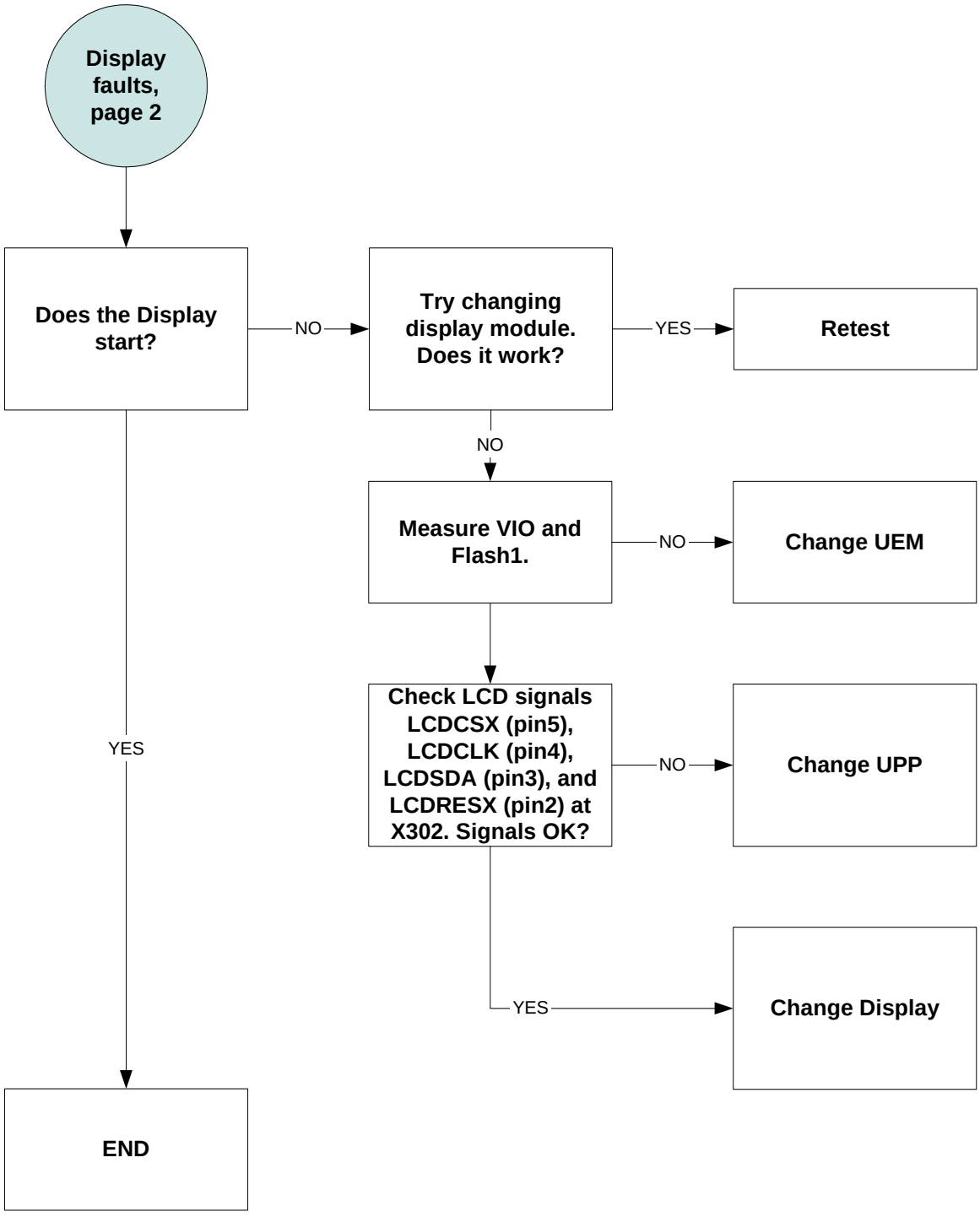



Audio faults, page 3
Is internal handsfree speaker (IHF) working?
NO
Select a ring tone and measure signals at L150 and L151. Is signal OK?
YES
Change B301
NO
Measure GenIO28. Is it OK (1.8V)?
NO
Change UPP
YES
Set the mobile terminal in Local Mode. Use Phoenix Troubleshooting > Phone Control > Phone State Tab > select Local Mode > Execute. Then use Audio test > HP microphone in/Ext Speaker out > Loop ON. To enable IHF turn on GenIO (10). Measure and check IHF testpoints J150, J151. Is it OK?
NO
Change IHF
YES
Change the UPP
YES
Audio faults, page 4

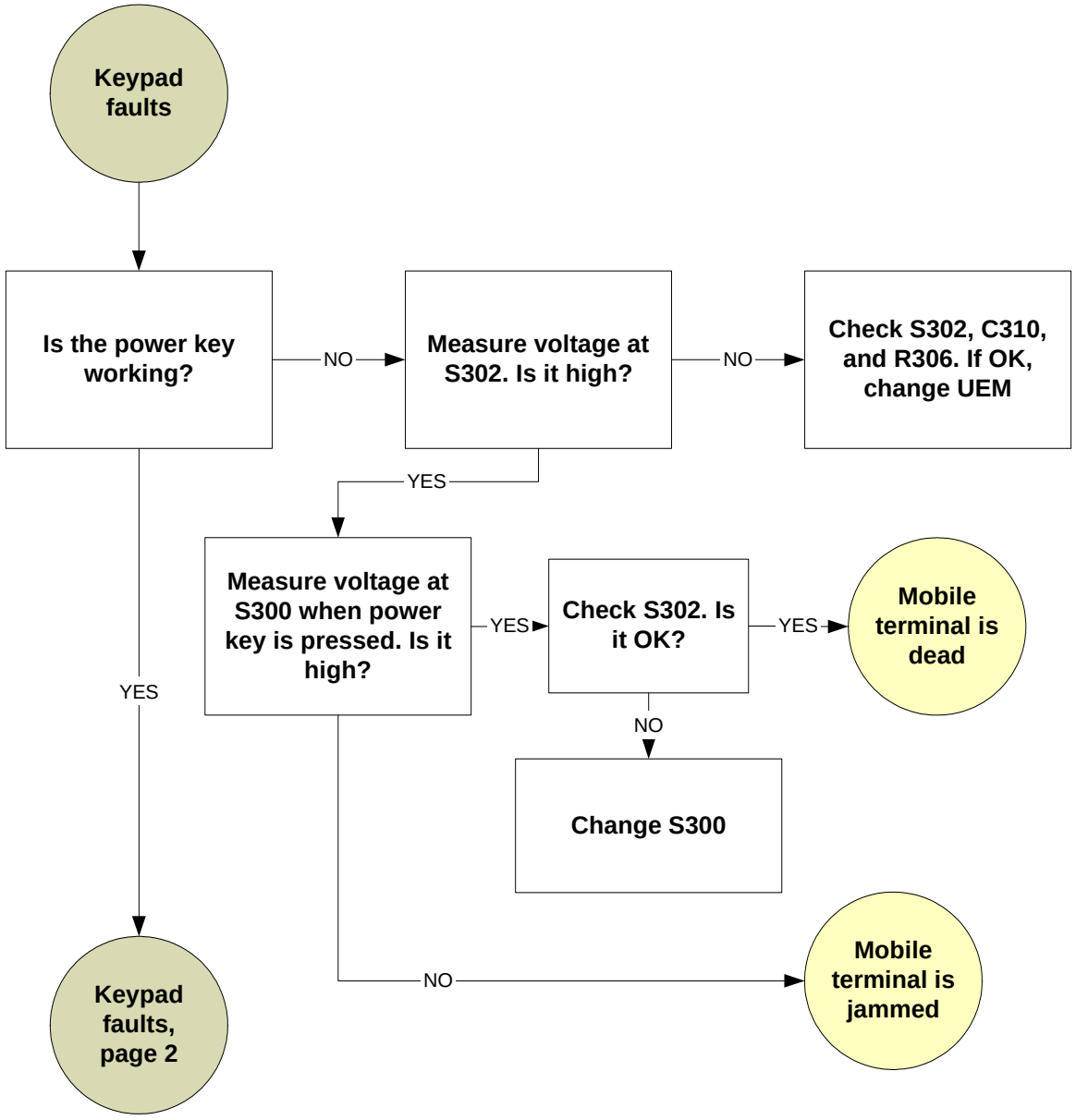


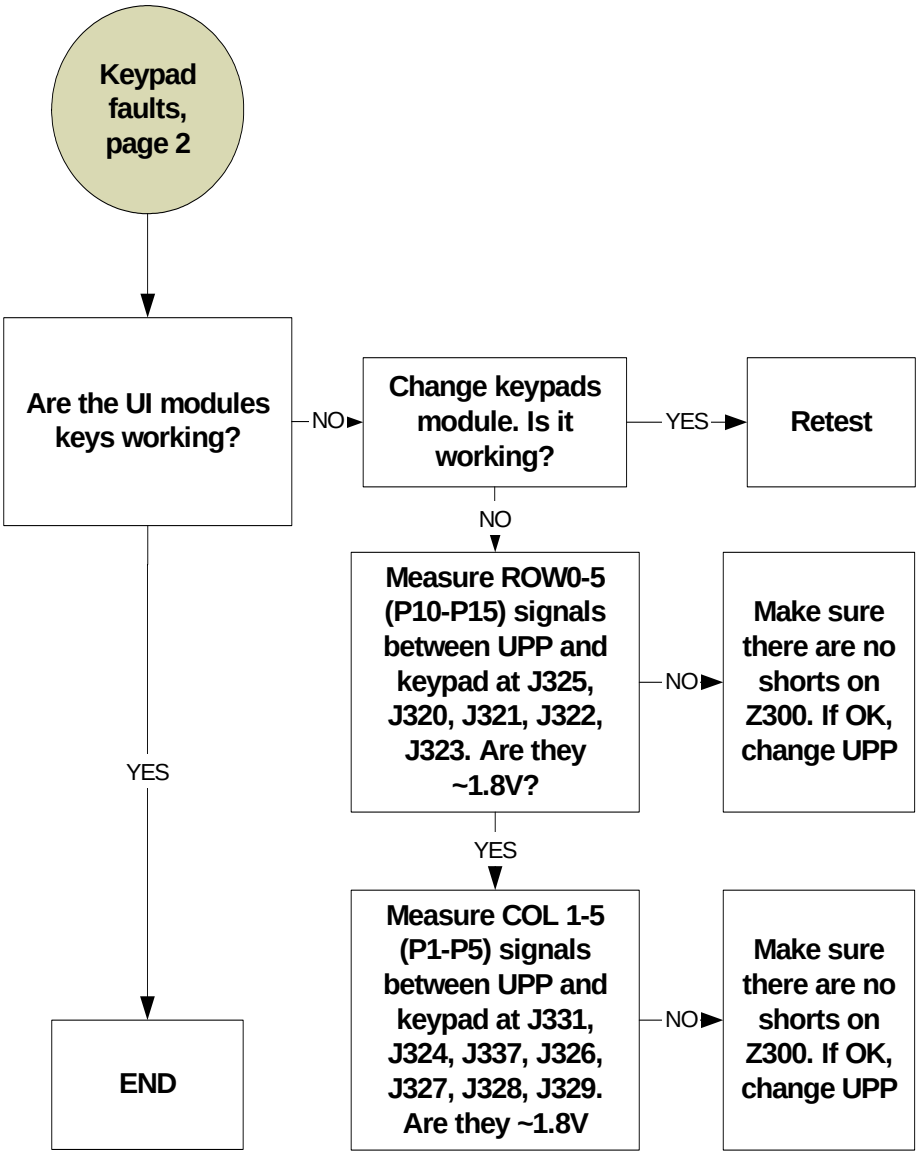
Display Faults



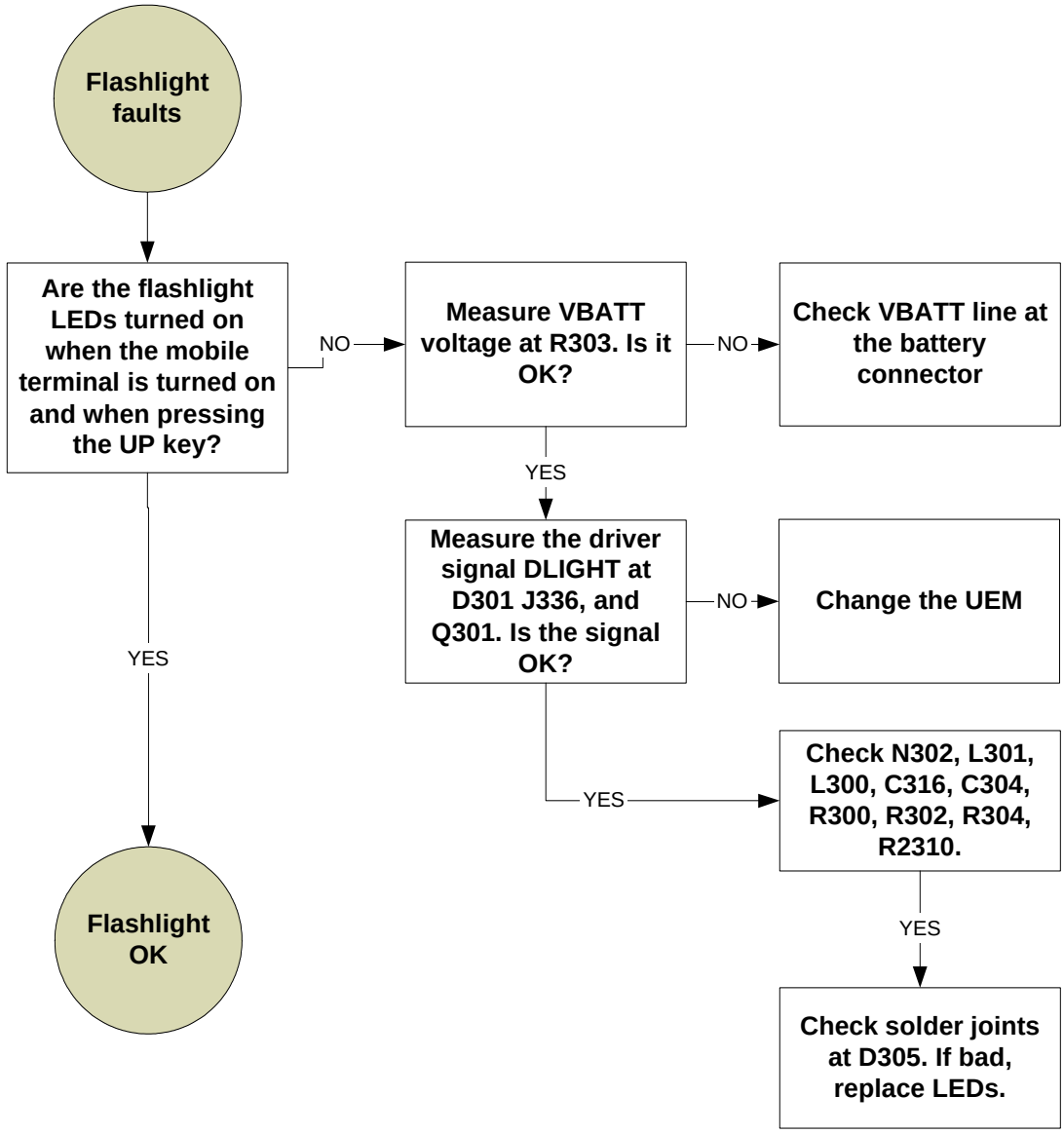


Keypad Faults





Flashlight


Flashlight faults
Are the flashlight LEDs turned on when the mobile terminal is turned on and when pressing the UP key?
NO
Measure VBATT voltage at R303. Is it OK?
NO
Check VBATT line at the battery connector
YES
Measure the driver signal DLIGHT at D301 J336, and Q301. Is the signal OK?
NO
Change the UEM
YES
Check N302, L301, L300, C316, C304, R300, R302, R304, R2310.
YES
Check solder joints at D305. If bad, replace LEDs.
YES
Flashlight OK

This page intentionally left blank.